

The first release of the LF3320 Horizontal Filter, Revision A, forces a configuration register writing dependency not documented in the data sheet. While this ordering dependency may no longer be required for future revisions of the LF3320, full compatibility with future releases will be maintained.

### Configuration Register Dependency

The LF3320 uses writable registers for configuration. The registers determine the various modes of operation for the device. Table 1 shows which registers are affected by the order dependency. The other configuration registers, as well as the coefficient registers, are not affected.

When configuring or re-configuring the LF3320, Configuration Register 5 must be written before writing either or both Configuration Register 1 and 3. Following this, Configuration Register 6 (undocumented register – Address 206H) must be written to properly configure the device. Listed below are various set up scenarios and the

proper sequence for writing these registers.

### Configuration Register Setup

Configuration Register 5 determines the basic operation of the LF3320. It sets the cascade, single/dual, and input/output modes. Since this register determines whether the part is in single or dual filter mode, it must be set before loading the registers which set up the I/D registers (Configuration Register 1 and 3).

In single filter mode, writing to Configuration Register 1 will configure both filters A and B. In dual filter mode, Filter A is set up by writing to Configuration Register 1 and Filter B is set up by writing to Configuration Register 3. As noted above, writing to either of these addresses should only take place after Configuration Register 5 has been written.

After writing Configuration Register 5, 1, and 3 (if needed), you must write to Configuration Register 6. This undocumented register location will force

the device into the mode set up by the other registers. Note that the device treats a write to Configuration Register 6 like any other configuration register loading. A data word (2nd word) is expected following the address (1st word). This data word should be 000H. Figure 1 shows a sequence for properly configuring the LF3320.

Future revisions of the LF3320 won't require writing Configuration Register 6. A write to this location will still reset the I/D register lengths (maintaining current code compatibility).

Configuration Registers 0, 2, and 4 can be written at any time and in any order. A write to Configuration Register 6 is not required when writing to any or all of these three registers.

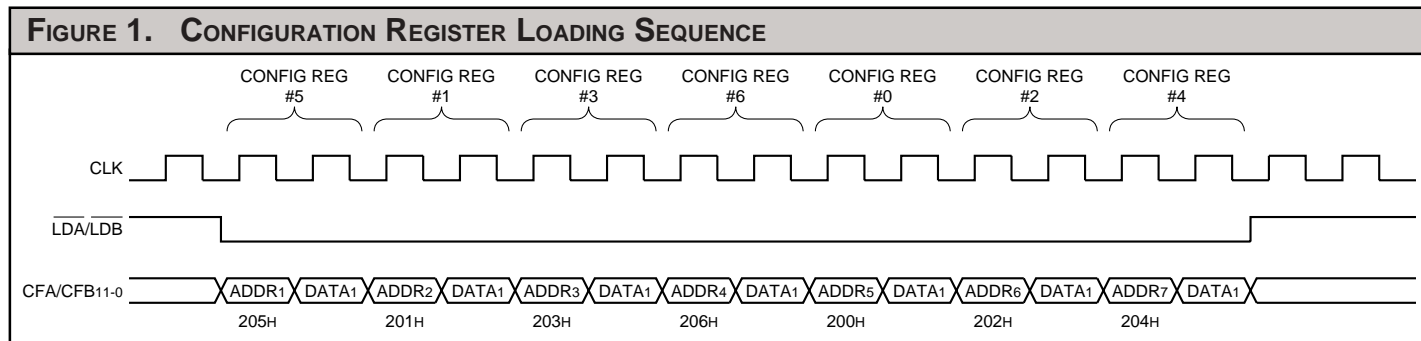
Please note, the above also applies when re-configuring Configuration Registers 1, 3, or 5.

### Configuration and I/D Registers Timing Dependency

When configuring or re-configuring the LF3320 there is a corresponding timing relationship between the Configuration Register and the I/D Registers; this timing dependency is related to the active level of SHEN $\bar{A}$  and SHEN $\bar{B}$ .

In order to assure correct operation, SHEN $\bar{A}$  and SHEN $\bar{B}$  must be held active for at least 'I/D length + 2' clock cycles after writing to the last Configuration Register (1, 3, or 6).

TABLE 1. AFFECTED CONFIGURATION REGISTERS	
REGISTERS	FUNCTIONAL DESCRIPTION
Config Reg 1 Address 201H	Filter A: Odd-tap Interleave, I/D Register Length, Even/Odd Taps, Data Reversal
Config Reg 3 Address 203H	Filter B: Odd-tap Interleave, I/D Register Length, Even/Odd Taps, Data Reversal
Config Reg 5 Address 205H	Cascaded Mode, Single/Dual Mode, Filter B Input, Output Adder Control



**Horizontal Digital Image Filter**

For example, in Single Filter Mode, an I/D length of 7 was loaded and Configuration Register 6 (address 206H) was the last register written.  $\overline{SHENA}$  and  $\overline{SHENB}$  must be held active, after the data write to Configuration Register 6, for at least 9 clock cycles ( $7 + 2 = 9$ ).

When in Dual Filter Mode,  $\overline{SHENA}$  needs only to be held active after a write to Configuration Register 1 or 6;  $\overline{SHENB}$  needs only to be held active after a write to Configuration Register 3 or 6. It is important to note that in Single Filter Mode, both  $\overline{SHENA}$  and  $\overline{SHENB}$  need to be held active for the same duration, 'I/D length + 2' clock cycles after writing to the last Configuration Register (1, 3, or 6); this is accomplished by simply connecting them together.

**LF Interface™**

Filter A and Filter B LF Interfaces™ are used to load data into the coefficient banks and the Configuration/Control

Registers.  $\overline{LDA}$  and  $\overline{LDB}$  are used to enable or disable the LF Interface™. A LOW input permits data loading; conversely, a HIGH disables the LF Interface™. When data is not being loaded into the LF Interface™,  $\overline{LDA}$  and  $\overline{LDB}$  should be inactive. In Dual Filter Mode data can be loaded through the LF Interface™; however,  $\overline{SHENA}$  must be held for the duration of 'I/D Register Length + 2' clock cycles from the data write to Configuration Registers 1 or 6, and  $\overline{SHENB}$  must be held for the duration of 'I/D Register Length + 2' clock cycles from the data write to Configuration Registers 3 or 6. As previously stated, in Single Filter Mode, both  $\overline{SHENA}$  and  $\overline{SHENB}$  need to be held active for the same duration, 'I/D length + 2' clock cycles after writing to the last Configuration Register (1,3, or 6); this is accomplished by simply connecting them together.

PAUSEA and PAUSEB are used to effectively slow the rate of loading data through the LF Interfaces™ when

interfacing with a microprocessor or controller. It is recommended that  $\overline{SHENA}$  and  $\overline{SHENB}$  be active when addressing their respective Configuration Registers and continue holding them LOW prior to the data write to their respective Configuration Registers. Once again,  $\overline{SHENA}$  and  $\overline{SHENB}$  must be held active for at least the 'I/D Register Length + 2' clock cycles from the data write to Configuration Registers 1, 3, or 6.

Performing a write to Configuration Registers 1, 3, or 6 first will decrease the active delay time of  $\overline{SHENA}$  and  $\overline{SHENB}$  when configuration or re-configuration involves more than one write to the Configuration/Control Registers. Meanwhile, when  $\overline{SHENA}$  and  $\overline{SHENB}$  are active, all remaining functions of the LF Interface™ are available.

Figure 2 shows the corresponding timing relationship between the Configuration Registers and the I/D Registers.

