

12Mbit Frame Buffer / FIFO

Providing designers with a single-chip approach to Sequential and Random Data Access

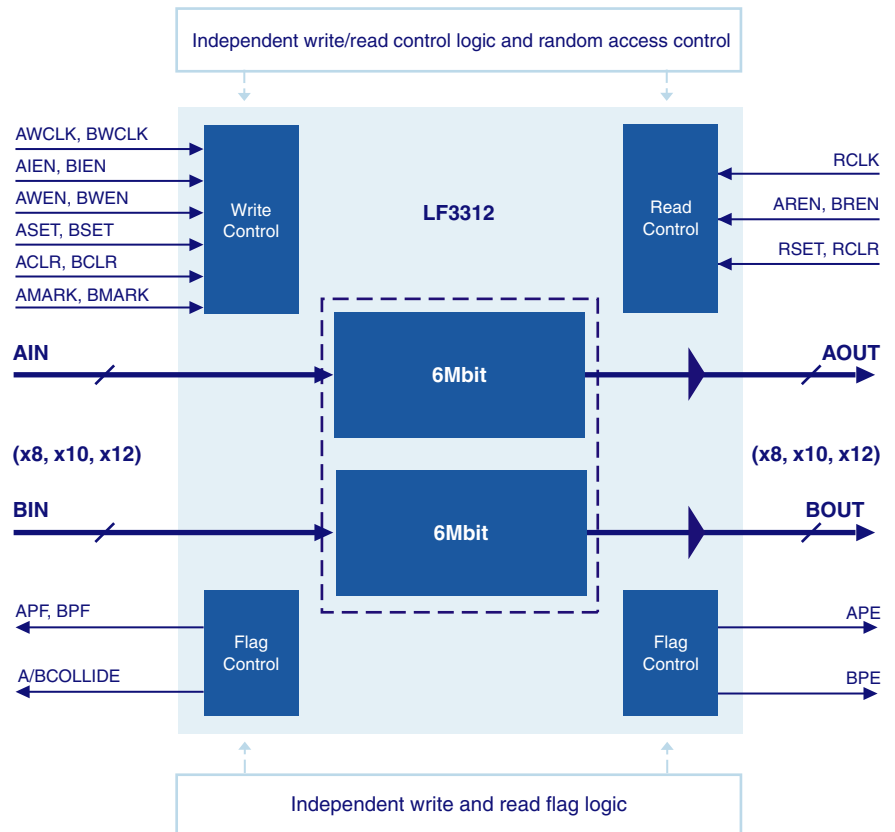
The LOGIC Devices LF3312 performs essential data / video buffering and reordering tasks common to systems that pass data between processing blocks. It leverages advanced embedded memory and addressing technologies to implement high-level storage functions traditionally comprised of smaller FIFOs or inflexible standard memory ICs and controllers. This off-the-shelf solution shortens design cycles, simplifies designs and reduces overall cost. A first-generation product, the LF3312 provides designers with a new, single-chip approach to both sequential and random data access. An ideal device for both video and communications / networking equipment where storage density, speed and flexible addressing is necessary.

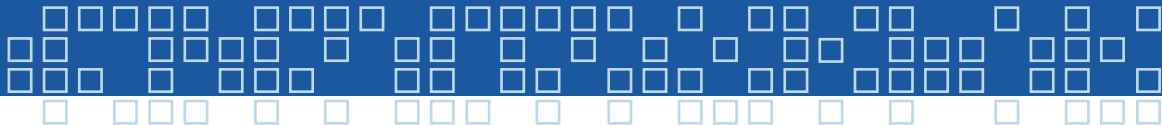
FEATURES:

- Configurable 12,441,600-bit Memory
 - Allocate as Single/Dual Channels
 - Selectable Input/Output Word Widths
- Up to 83Mhz Operation of Clocks
- Random Access Modes
 - Random Write/Sequential Read
 - Sequential Write/Random Read
 - Seamless Address Space is Achieved with Cascaded Devices
- FIFO Modes
 - Independent W/R Clocks
 - Independent W/R Pointer Resets
 - Programmable Near-Full/Empty Flags
 - Synchronous Shift Register Mode
 - Cascade Devices for Depth Expansion
- ITU-R 656 TRS Detect/Synchronize
- Control Interfaces
 - I²C Two-Wire Interface
 - Parallel MPU Interface
- Input Enable (Write Mask)
- Output Enable (Data Skipping)
- 172 ball LPGA
- 1.8V Internal Power Supply
- 3.3V I/O Supply

MEMORY ALLOCATION:

- 1,555,200 x 8-bit (single channel)
- 1,244,160 x 10-bit (single channel)
- 1,036,800 x 12-bit (single channel)
- 777,600 x 16-bit (single channel)
- 622,080 x 20-bit (single channel)
- 518,400 x 24-bit (single channel)
- 777,600 x 8-bit x 2 (dual channel)
- 622,080 x 10-bit x 2 (dual channel)
- 518,400 x 12-bit x 2 (dual channel)

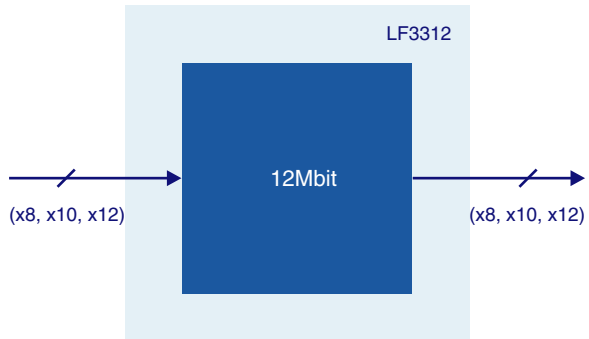
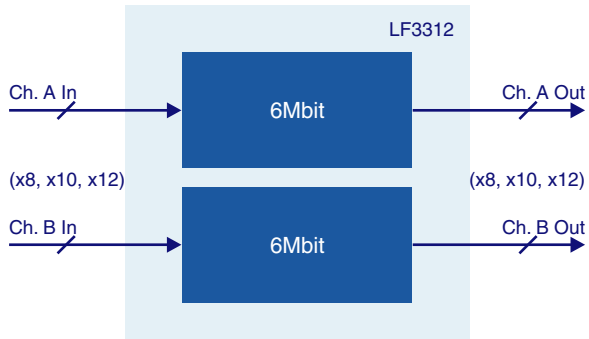
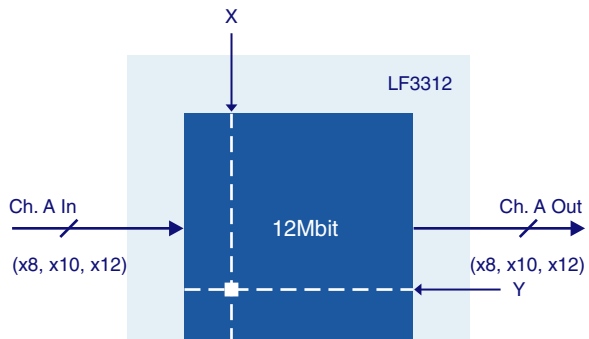




Configurations

Modes

Applications

Configurations	Modes	Applications
<p>Single Channel</p> 	<ul style="list-style-type: none"> ❑ One Deep FIFO w/ Async. R/W Controls ❑ One Deep Synchronous Shift Register 	<ul style="list-style-type: none"> ❑ HDTV field & frame store ❑ SDTV frame store ❑ Video delay line ❑ Data buffering across clock domains ❑ Motion detection ❑ Scan rate converters
<p>Dual Channel</p> 	<ul style="list-style-type: none"> ❑ Two Independent FIFOs w/ Async. R/W Controls ❑ Two Synchronous Shift Registers ❑ Independent FIFO & Shift Register - Ch.A sync to Ch.B 	<ul style="list-style-type: none"> ❑ Frame Synchronizer ❑ TBC (Time Base Correction) ❑ Synchronizing multiple video/data feeds ❑ De-interlacing ❑ Parallel buffering of multiple data streams ❑ CCTV and security camera systems
<p>Random Access</p> 	<ul style="list-style-type: none"> ❑ Random Access Write with Sequential Read ❑ Random Access Read with Sequential Write 	<ul style="list-style-type: none"> ❑ PIP or POP video display ❑ CCD/CMOS image sensor buffer ❑ Machine Vision: Region of Interest ❑ Real-time video compression buffer ❑ Image rotation or zoom