

## 24Mbit Frame Buffer / FIFO

*Leading the Way with the Industry's Highest Density FIFO*

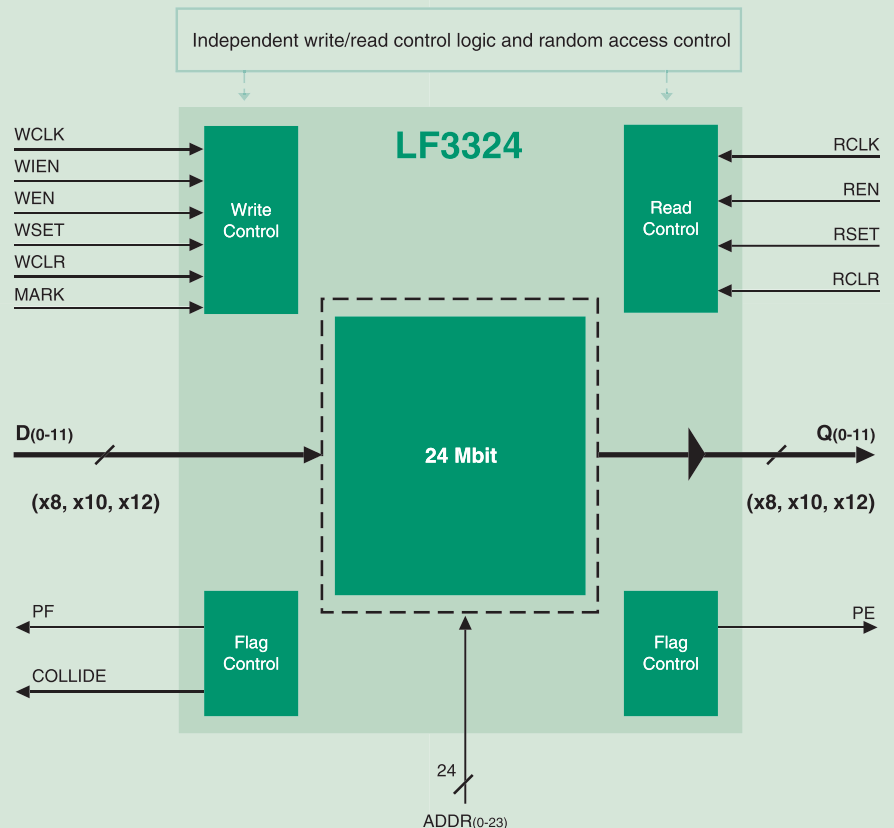
*This Next-Generation Buffer performs essential data / video buffering and reordering tasks common to systems that pass data between processing blocks. It leverages advanced embedded memory and addressing technologies to implement high-level storage functions traditionally comprised of smaller FIFOs or inflexible standard memory ICs and controllers. This off-the-shelf solution shortens design cycles, simplifies designs and reduces overall cost. An ideal device for both video and communications / networking equipment where storage density, speed and flexible addressing is necessary.*

### FEATURES:

- Configurable **24,883,200-bit Memory**
  - **Configurable I/O Word Widths**
- Up to **74Mhz** Operation of Clocks
- **Random Access Modes**
  - Random Write/Sequential Read
  - Sequential Write/Random Read
  - **2-D Image Address Space option**
  - Maintain a **Seamless Address Space with Cascaded Devices**
- **FIFO Modes**
  - Independent W/R Clocks
  - Independent W/R Pointer Resets
  - Programmable Near-Full/Empty Flags
  - Synchronous Shift Register Mode
  - **Cascade Devices for Depth Expansion**
- **ITU-R 656 TRS Detect/Synchronize**
- Control Interfaces
  - **I<sup>2</sup>C Two-Wire Interface**
  - Parallel MPU Interface
- Input Enable (Write Mask)
- Output Enable (Data Skipping)
- **172 ball LPGA**
- 1.8V Internal Power Supply
- 3.3V I/O Supply

### MEMORY ORGANIZATION:

- 3,110,400 x 8-bit
- 2,488,320 x 10-bit
- 2,073,600 x 12-bit





## Configurations

## Modes

## Applications

<p><b>Random Access</b></p> <p>24Mbit</p> <p>Programmable Horiz. Resolution</p>	<ul style="list-style-type: none"> <li>❑ 2-D Address Space option for simplified image access</li> <li>❑ Random Access Write with Sequential Read</li> <li>❑ Random Access Read with Sequential Write</li> </ul>	<ul style="list-style-type: none"> <li>❑ PIP or POP video display</li> <li>❑ CCD/CMOS image sensor buffer</li> <li>❑ Machine Vision: Region of Interest</li> <li>❑ Real-time video compression buffer</li> <li>❑ Image rotation or zoom</li> </ul>
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<p><b>FIFO</b></p> <p>24Mbit</p>	<ul style="list-style-type: none"> <li>❑ Deep FIFO w/ Async. R/W Controls</li> <li>❑ One Deep Synchronous Shift Register</li> </ul>	<ul style="list-style-type: none"> <li>❑ Frame Synchronizer</li> <li>❑ HDTV field &amp; frame store</li> <li>❑ SDTV frame store</li> <li>❑ Video delay line</li> <li>❑ Data buffering across clock domains</li> <li>❑ Motion detection</li> <li>❑ Scan rate converters</li> <li>❑ TBC (Time Base Correction)</li> <li>❑ Synchronizing multiple video/data feeds</li> <li>❑ De-interlacing</li> </ul>
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*Technological Leadership  
through Engineering Excellence*

