

Using Data Bypass

Overview

The data bypass mode on the LF3370 allows user data to be passed through the part without altering its value. The bypass block can be visualized as four FIFOs bridging the input and output multiplexers. It is important to note that the bypass RAM is always reading data from the input demultiplexer. The state of the DATAPASS pin does not enable or disable the RAM. Instead, it simply directs delayed input data directly to the output, as described below.

Delay Calculation

For most applications to properly use the data bypass block, it is important that we match its delay with that of the core – so that a seamless bypass path is established. There are three factors that affect the total data bypass delay. These are the input delay, data bypass delay and the output delay. The length of each section will vary with the current part configuration and I/O format. The total delay (from data input to data output) is the sum of all three delays.

To calculate the delay through the input demultiplexer the clock rate at the input section and the input format must be considered. The input clock rate can be determined by referencing Table A. Next, the delay through the demultiplexer must also be established. This can be found in the LF3370 data sheet (under the Input Demultiplexer section on page 5). If the input section clock rate is CLK/2, then the delay through the demultiplexer must be doubled.

The output delay is more easily calculated. The standard delay through the output section is two clock cycles. If the output multiplexer clock frequency from Table A is CLK/2, then the output multiplexer delay is doubled (to 4).

Table A. Internal Clock Speeds				
Input*	Output*	Input DEMUX	Core	Output MUX
3 Channel	3 Channel	CLK	CLK	CLK
3 Channel	2 Channel	CLK	CLK	CLK
3 Channel	1 Channel	CLK/2	CLK/2	CLK
2 Channel	3 Channel	CLK	CLK	CLK
2 Channel	2 Channel	N/A	N/A	N/A
2 Channel	1 Channel	N/A	N/A	N/A
1 Channel	3 Channel	CLK	CLK/2	CLK/2
1 Channel	2 Channel	N/A	N/A	N/A
1 Channel	1 Channel	N/A	N/A	N/A

*Key Channel is not Considered

Delay Calculation Cont'd

Finally, the bypass RAM delay must be calculated. The bypass RAM always runs at the external clock frequency. If the core clock frequency from Table A is CLK/2 the data will travel through the bypass RAM twice as fast as the data in the core. In this case it may be desirable to double the bypass length to synchronize the data flow. The bypass length is equal to the delay in configuration register 202H plus two. When the length of the bypass RAM is altered, all data in the RAM is reset. Thus, after resetting the bypass length, the RAM must be fully reloaded before usable data is available. Note that the delay length loaded in 202H is applied to each separate bypass RAM (i.e. all paths have the same length).

The formula for total delay is: $D_{TOTAL} (CLK) = D_{IN} + D_{DATAPASS} + D_{OUT}$

Timing and Formatting Considerations

Before implementing data bypass, there are a few timing and formatting considerations that must be observed. First, note that any formatting performed by the input or output de/multiplexer is applied to both core and bypass data. That is, if data is being input in 4:2:2 multiplexed on two channels and the output is being formatted to three channel non-interleaved format, bypassed data is de-multiplexed by the input section and then treated as three channel output by the output section. Similarly, if the bypass data consisted of a serial stream of data at the input, the output data would be spread over three channels.

Next, if configuration register 201H, bits 7 or 8 are set, the 'W' channel output will be not be mapped to the 'A' channel data bypass path. For example, if configuration register 201H, bits 7 and 8 were set to 11b, the 'D' (or Key) channel will be replace the 'A' channel bypass output while DATAPASS is enabled. This will not, however, place the 'A' channel bypass data onto the 'D' channel. It does not swap the two the channels, it merely overwrites the 'W' channel.

In some unsupported modes, where input and output format are both 4:2:2, if the core bypass RAM length is not equal to the length of the core data path, the output synchronization signal (if used) may become corrupted. Thus, when the data bypass mode is lifted, the output will need to be resynchronized. This is accomplished by bringing the SYNC signal LOW at the appropriate time (see LF3370 Datasheet).

Finally, the timing from the DATAPASS pin to the output should be noted. As can be seen in Figure 1, the DATAPASS pin must be brought LOW two cycles before bypass data is desired on the output. It is important to note that the output multiplexer may be running at CLK/2 rate when the input format is 4:2:2 interleaved on a single-channel and the output is three-channel non-interleaved format. If this is the case, the DATAPASS register and the two data path registers in the output section will be running at the divided clock speed. This will make the output multiplexer appear to be four clock cycles long. For this reason it is important to be aware of the internal clock frequency of the output multiplexer. The DATAPASS signal must be brought HIGH on the internal clock's rising edge.

Typical Core Delay

A typical functional arrangement consisting of three input channels, three output channels, and a matrix to half band filter data path, would exhibit a core delay of the following:

$$1(\text{input bias adder}) + 2(\text{gamma}) + 6(\text{matrix}) + 35 (\text{halfband}) + 2(\text{gamma}) + 1 (\text{output bias adder}) - 2(\text{internal bypass ram delays}) = 45 \text{ or '2D' Hex.}$$

In this case, Configuration Register 202H (bypass length) should be loaded with '2D' Hex.

