

Clock and Data Synchronization

Overview

Depending on the operating mode, the LF3370 may require both clock and data synchronization. In a mode that requires the LF3370 to deal with interleaved or multiplexed data, halving the clock rate of one or more of the internal blocks may be necessary. When there are multiple clock domains involved in a particular mode of operation, the different clock domains need to be synchronized together. Thus, unless both the input and output data are in non-interleaved (three channel) mode, some form of data synchronization will be necessary to properly interleave or de-interleave the data. This is achieved by using the $\overline{\text{RESET}}$ signal. If interleaved output data is desired, an output synchronization signal $\overline{\text{SYNC}}$ will be provided. Conversely, if the LF3370 takes interleaved data as its input, an input synchronization signal $\overline{\text{SYNC}}$ must be provided.

Clock Synchronization

The LF3370 can operate in modes where the clock rate provided to certain internal sections will be half of the external clock rate. To determine if a half-clock-rate (CLK/2) condition exists under a particular configuration, thus requiring clock synchronization, Table A should be consulted. If any of the internal sections require CLK/2, then synchronization is required. Without proper synchronization, it is impossible to determine if the CLK/2 signal is locked to the even or odd cycle of CLK (see Figure 1).

When the part is initially powered up, the first register that should be set is 200H. The contents of this register determine the I/O format and thus determine the clock speed requirements for each internal block of the chip. Table A may be referred, to determine if any block will be running at CLK/2. The LF Interface™ never runs at the CLK/2 rate, that is, it runs at the external CLK rate at all times.

After the internal clock dividers are setup, a $\overline{\text{RESET}}$ cycle must occur. To properly align all of the internal clocks, pull $\overline{\text{RESET}}$ LOW for at least one cycle. Any information in the data path will be compromised if a $\overline{\text{RESET}}$ event takes place. Two cycles after the $\overline{\text{RESET}}$ is returned HIGH, the internal clocks will be synchronized with the external clock (see Figure 2).

It is very important to note that changing the state of the clock dividers (setting configuration register 200H) during circuit operation will invalidate any data currently in the data path. After setting 200H one external cycle should be allowed to pass before a $\overline{\text{RESET}}$ pulse.

Table A. Internal Clock Speeds				
Input*	Output*	Input DEMUX	Core	Output MUX
3 Channel	3 Channel	CLK	CLK	CLK
3 Channel	2 Channel	CLK	CLK	CLK
3 Channel	1 Channel	CLK/2	CLK/2	CLK
2 Channel	3 Channel	CLK	CLK	CLK
2 Channel	2 Channel	N/A	N/A	N/A
2 Channel	1 Channel	N/A	N/A	N/A
1 Channel	3 Channel	CLK	CLK/2	CLK/2
1 Channel	2 Channel	N/A	N/A	N/A
1 Channel	1 Channel	N/A	N/A	N/A

*Key Channel is not Considered

Input Data Synchronization

If the input format is set to three channel (generally, 4:4:4 non-interleaved) then input data synchronization is not necessary and SYNC should be held in a steady state (logic HIGH or LOW). Otherwise, input synchronization is required. Input synchronization assumes that this input signal is in 4:2:2 interleaved format. This is applicable to formats such as orthogonally sampled 4:2:2 YCbCr video. The LF3370 Datasheet shows examples of input synchronization for 4:2:2 input data multiplexed onto one or two channels.

Once the input data is synchronized by bringing the $\overline{\text{SYNC}}$ LOW to flag a particular input word, the LF3370 will maintain synchronization autonomously. If the input data streams shifts from the original synchronization, SYNC must be brought LOW again to re-synchronize the data. Thus, after a horizontal or vertical retrace when an odd length of data may be encountered, another SYNC signal must be issued.

The SYNC signal cannot be used to skew the input data in time. As can be seen in Figure 3, moving the SYNC pulse will not simply shift the input channels. However, this does effectively prevent information from being accurately represented by the data stream. This is generally undesirable for most applications.

Please note that Figure 3 shows various possible ways that data synchronization can be achieved. It is recommended that one method be used consistently.

The $\overline{\text{SYNC}}$ signal must occur on the data word that is to be multiplexed onto the B-Channel (or Cb sample) in 4:2:2 format (Figure 3). If invalid data (e.g. non-video information) is presented at the input, the part will need to have another SYNC strobe to realign the input and output data synchronization signals.

*NOTE: In a mode of operation that requires CLK/2, the synchronizing LOW on $\overline{\text{SYNC}}$ must be coincident with a rising edge of both CLK and CLK/2.

Output Data Synchronization

If the output data is to be interleaved in a 4:2:2 format (output multiplexed onto one or two channels) then a synchronization pulse will be provided. Since the Y-channel is not used in any mode that would require output synchronization, the Y-channel's LSB serves as an output synchronizer. Whenever there is a valid B-channel output (Cb in YCbCr format), the Y[0] pin will be pulled LOW. Any data output pins not being used in a given mode will be driven to a LOW state.

While input data synchronization is not required for three channel input, the $\overline{\text{SYNC}}$ signal must be pulled LOW for the first valid point of data if the output data requires synchronization.

If the part is in a mode where output synchronization is required and core bypass is initiated, the output synchronization may become incorrect if the core bypass RAM length is not equal to the length of the data path through the core.

