Application Note
Discrete Cosine Transform with the LF3320

The fundamental processing step at the heart of the discrete cosine transform (DCT) based block coding scheme is the mathematical operation of matrix multiplication, a mode of operation supported by the LF3320 Horizontal Digital Image Filter.

A video image can be broken into N by N blocks of picture elements, joining end-to-end across the x and y dimensions of a complete image. The N by N block of spatial information is transformed into the frequency domain by performing a Forward DCT (FDCT) on each N by N block of pixel information.

The N by N block of DCT coefficients represent relative amounts of spatial frequencies from the original input data (see Figure 1). A reversal of the FDCT process transforms the DCT coefficients from the frequency domain back to the spatial domain, referred to as, the Inverse DCT (IDCT).

The mathematical representations of the 2-D FDCT and the 2-D IDCT are represented in Figure 2. An important property of the two dimensional DCT is the separability into one dimension for each of the columns and rows (see Figure 3 and 4); represented in matrix form, the mathematical operation is simplified (see Figure 5). As a result, the overall hardware requirements are simplified into a single-chip solution.

This application note describes how to configure the LF3320 Horizontal Digital Image Filter to perform matrix-vector multiplication for the purpose of DCT based block coding. It is assumed the reader is familiar with operation of the device and certain aspects of Block Transform coding. Please refer to the data sheet for more specific device information; for further reference on DCT Block Based Coding, Martucci, S., "*Symmetric Convolution and the Discrete Sine and Cosine Transforms,*" IEEE Trans. Signal Proc., vol. 42 pp. 1038-1051, May 1994.

FIGURE 1. N x N BLOCKS OF PIXEL DATA

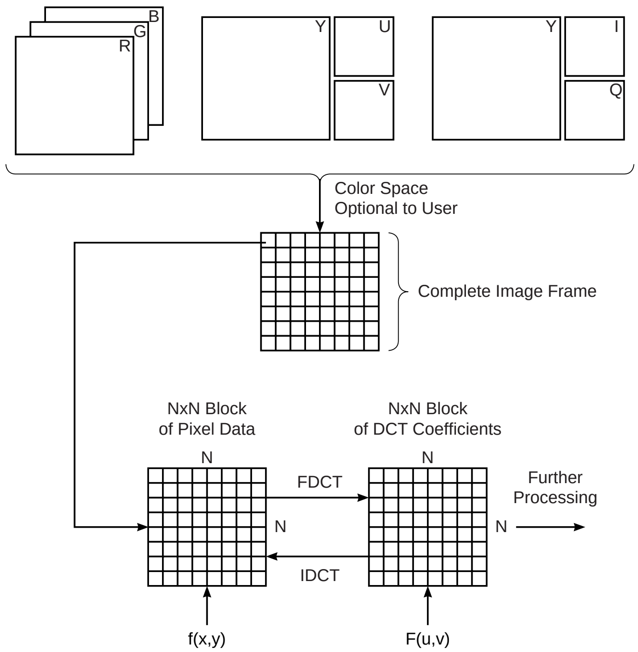


FIGURE 2. 2-D DCT EQUATIONS

Forward DCT:

$$F(u,v) = C(u)C(v)\left[\sum_{x=0}^{(N-1)}\sum_{y=0}^{(N-1)} f(x,y)\cos\frac{(2x+1)u\pi}{2N}\cos\frac{(2y+1)v\pi}{2N}\right]$$

Inverse DCT:

$$f(x,y) = \left[\sum_{u=0}^{(N-1)}\sum_{v=0}^{(N-1)} C(u)C(v)F(u,v)\cos\frac{(2x+1)u\pi}{2N}\cos\frac{(2y+1)v\pi}{2N}\right]$$

where: $C(u) = \frac{1}{\sqrt{N}}$, $C(v) = \frac{1}{\sqrt{N}}$ for u,v = 0;

$C(u) = \sqrt{\frac{2}{N}}$, $C(v) = \sqrt{\frac{2}{N}}$ for u,v = 1 through N-1;

N = 8 or 16

LF3320 Role in DCT

The LF3320 is capable of computing both the FDCT and the IDCT for 8 x 8 or 16 x 16 blocks of data at rates up to 83 MHz. Following the one-dimensional (1-D) theoretical equations for an 8 by 8 DCT, a straightforward 1-D DCT will require 64 multiplications and 56 additions. Subsequently, a straightforward two-dimensional (2-D) 8 by 8 DCT will require 1024 multiplications and 896 additions. When configured for matrix-vector multiplication the LF3320 is capable of supporting the computational requirements for a straightforward 8 by 8 DCT in just 768 ns.

FIGURE 3. 1-D DCT BLOCK BREAK DOWN

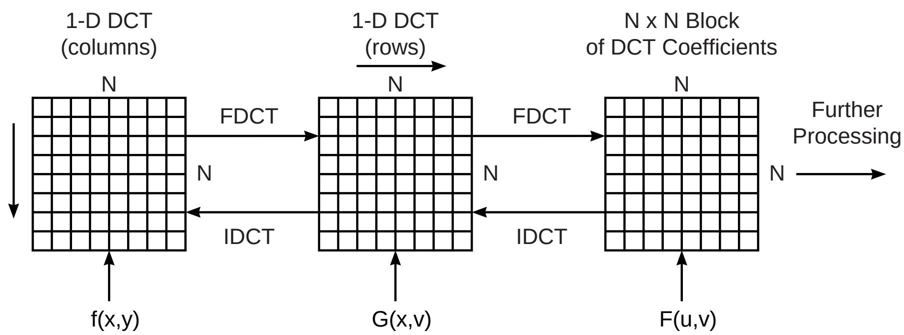


FIGURE 4. 1-D DCT EQUATIONS

$$F(u,v) = C(u)\left[\sum_{x=0}^{(N-1)} G(x,v)\cos\frac{(2x+1)u\pi}{2N}\right]$$

$$G(x,v) = C(v)\left[\sum_{y=0}^{(N-1)} f(x,y)\cos\frac{(2y+1)v\pi}{2N}\right]$$

where: $C(u) = \frac{1}{\sqrt{N}}$, $C(v) = \frac{1}{\sqrt{N}}$ for u,v = 0;

$C(u) = \sqrt{\frac{2}{N}}$, $C(v) = \sqrt{\frac{2}{N}}$ for u,v = 1 through N-1;

N = 8 or 16

FIGURE 5. 1-D DCT EQUATIONS IN MATRIX FORM

$$D(u,v) = \begin{cases} \frac{1}{\sqrt{N}} & v = 0,\ 0 \le u \le N-1 \\ \sqrt{\frac{2}{N}}\cos\frac{(2v+1)u\pi}{2N} & 1 \le v \le N-1,\ 0 \le u \le N-1 \end{cases}$$

Let X = N x N Block of Pixel Data

Forward DCT: $Y = DXD^t$

Inverse DCT: $X = D^tYD$

In dual filter mode, Filter A will correspond with the rows or columns and Filter B will correspond with the columns or rows. In single filter mode, the LF3320 is capable of supporting a straightforward 16 by 16 DCT. To implement the 16 by 16 DCT, two devices are required, one each for the rows and columns.

Processing the DCT

When configured for matrix-vector multiplication, the LF3320 will perform 2N number of matrix-vector multiplications to realize a complete N by N DCT. The user is required to pre-load, as described in the device data sheet, N number of coefficient sets, containing N number of coefficients, into the coefficient memory banks, to satisfy both one dimensional matrix-vector operations (see Figure 4 and Figure 5).

Using the equations in Figure 5, the user can generate a DCT matrix of the required DCT dimension (i.e. filter coefficients). A simple program can be coded to accomplish this task; an example has been provided in Figure 10.

Each individual 12-bit coefficient, contained in the coefficient sets, is a representation from the DCT matrix (see Figure 6). That is to say, to perform floating-point arithmetic with fixed-point architecture, the DCT coefficients must be scaled and quantized (see Figure 7). The exponent for each coefficient will be of the same magnitude and sign. Two examples have been provided in Figure 11.

In Dual Filter mode, Filter A and Filter B will each have a maximum of 8 coefficient sets, corresponding to an 8 by 8 square matrix. In Single Filter mode, the filter will have a maximum of 16 coefficient sets, corresponding to a 16 by 16 square matrix. The multiplication of two square matrices will be performed as N number of matrix-vector multiplications.

This is accomplished by addressing each coefficient set, on each new clock cycle, while holding the current input

FIGURE 6. 8 x 8 DCT MATRIX - COSINE BASIS FUNCTION

D =

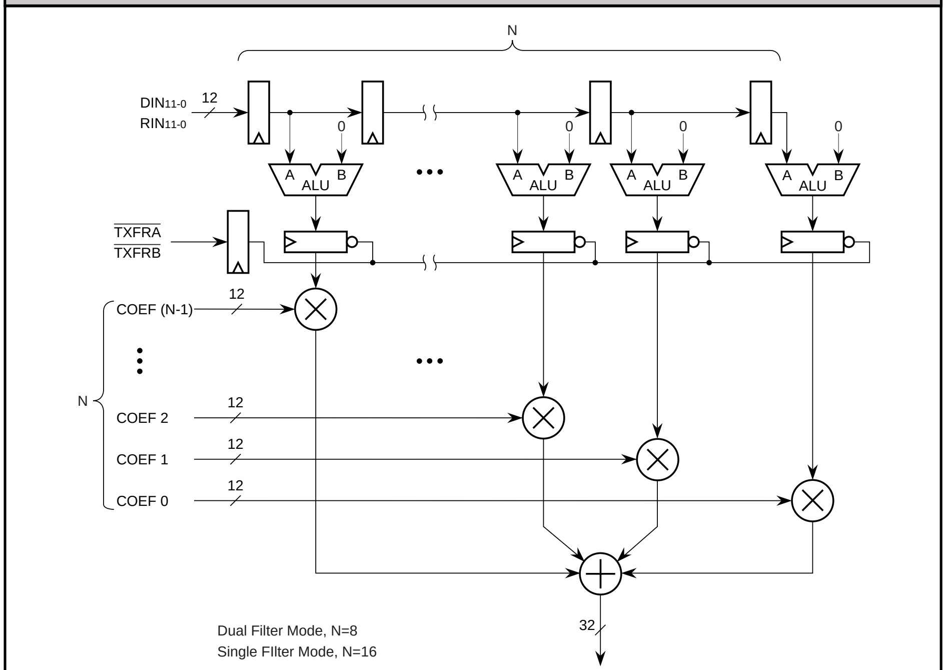
0.3536	0.3536	0.3536	0.3536	0.3536	0.3536	0.3536	0.3536
0.4904	0.1913	0.2778	0.0975	-0.0975	-0.2778	-0.4157	-0.4904
0.4619	0.4157	-0.1913	-0.4619	-0.4619	-0.1913	0.1913	0.4619
0.4157	-0.0975	-0.4904	-0.2778	0.2778	0.4904	0.0975	-0.4157
0.3536	-0.3536	-0.3536	0.3536	0.3536	-0.3536	-0.3536	0.3536
0.1913	-0.4904	0.0975	0.4157	-0.4157	-0.0975	0.4904	-0.2778
0.2778	-0.4619	0.4619	-0.1913	-0.1913	0.4619	-0.4619	0.1913
0.0975	-0.2778	0.4157	-0.4904	0.4904	-0.4157	0.2778	-0.0975

FIGURE 7. 8 x 8 DCT MATRIX - QUANTIZED COEFFICIENTS

D =

2D4H	2D4H	2D4H	2D4H	2D4H	2D4H	2D4H	2D4H
3ECH	353H	239H	0C8H	F38H	DC7H	CADH	C14H
3B2H	188H	E78H	C4EH	C4EH	E78H	188H	3B2H
353H	F38H	C14H	DC7H	239H	3ECH	0C8H	CADH
2D4H	D2CH	D2CH	2D4H	2D4H	D2CH	D2CH	2D4H
239H	C14H	0C8H	353H	CADH	F38H	3ECH	DC7H
188H	C4EH	3B2H	E78H	E78H	3B2H	C4EH	188H
0C8H	DC7H	353H	C14H	3ECH	CADH	239H	F38H

FIGURE 8. MATRIX-VECTOR MULTIPLY MODE



data-vector for N number of clock cycles. While processing the current data-vector, a new data-vector is loaded. This key feature of the LF3320, offers the user the ability to continuously process DCT results without pausing the input data stream. Once the pipeline is full, a DCT result is realized at the output on every clock cycle.

The LF3320 accepts 12-bit inputs and generates 16-bit outputs. The data is accepted and generated in raster order within the x and y dimensions of the block size (two's complement). Internal bit precision can grow to 32-bits. The full range of 32-bits is available to the user through use of the Round / Select / Limit circuitry (RSL circuitry). This will

FIGURE 9. MATRIX EQUATION

C = COEFFICIENTS
D = DATA INPUT
R = DATA OUTPUT

$$\begin{bmatrix} R_0 \\ R_1 \\ R_2 \\ \vdots \\ R_i \end{bmatrix} = \begin{bmatrix} C_{00} & C_{01} & C_{02} & \cdots & C_{0j} \\ C_{10} & C_{11} & C_{12} & \cdots & C_{1j} \\ C_{20} & C_{21} & C_{22} & \cdots & C_{2j} \\ \vdots & & & & \vdots \\ C_{i0} & C_{i1} & C_{i2} & \cdots & C_{ij} \end{bmatrix} \bullet \begin{bmatrix} D_0 \\ D_1 \\ D_2 \\ \vdots \\ D_i \end{bmatrix}$$

$$\left[R_i\right] = \sum_{i=0}^{(N-1)} \left[C_{ij} \bullet D_i\right]$$

For j=0,1,2,...,(N-1)
N=8 or 16

provide additional flexibility for both 8-point and 16-point DCTs. The 16-bit DCT output data can be manipulated to correspond with the 12-bit filter input data (see LF3320 data sheet). In addition to, but not with in the scope of this application note, the RSL circuitry can be used to perform quantization, of the final DCT output.

For an 8-point DCT, the Filter A output DOUT15-0 will become the Filter B input RIN11-0. The final 16-bit output will appear at ROUT3-0 / COUT11-0.

For a 16-point DCT, the output DOUT15-0 of the first device will become the input DIN11-0 to the second device. The final 16-bit output will appear at DOUT15-0 of the second device.

Matrix-vector Multiply Mode

In this mode, the LF3320 can be configured to multiply a square matrix of maximum size N (N = 8 or 16) by a column-vector of maximum size [8,1] or [16,1] (see Figure 8). The mathematical representation for this operation is in Figure 9.

When configured in the dual filter mode, the LF3320 can process two matrix-vector multiplications simultaneously (i.e. [8x8][8x1]). In the single filter mode, the LF3320 can process a single matrix-vector multiplcations (i.e. [16x16][16x1]).

When configuring the LF3320 for an [8x8][8x1] matrix operation, the coefficient banks will require 8 coefficient sets to be loaded into the coefficient memory banks; each coefficient set will have 8, 12-bit coefficients. The input data, [8x1] column-vector, will be loaded through DIN11-0 for Filter A. The Filter A output result, from the first 1-D DCT, will be loaded through RIN11-0, for the second 1-D DCT, of Filter B.

Conversely, when configured for a [16x16][16x1] matrix operation, the coefficient banks will require 16 coefficient sets to be loaded into the coefficient memory banks; each coefficient set will have 16, 12-bit coefficients. The input data, [16x1] column-vector, will be loaded through DIN11-0.

Mode Configuration

To configure the LF3320 for matrix-vector multiplication, bit 4 of Configuration Register 5 must be set to 1 (see Table 7). The configuration for single filter mode or dual filter mode will still apply (see device data sheet). Writing 012H (Filter B input RIN11-0) to Configuration Register 5 will configure the device for dual filter mode, [8x8][8x1] matrix-vector multiplication. Subsequently, writing 010H to Configuration Register 5 will configure the device for single filter mode, [16x16][16x1]matrix-vector multiplication.

Special Consideration

Some functions of the LF3320 must be disabled when configured for matrix-vector multiplication. This will apply to both the single filter mode and the dual filter mode; these functions are data reversal and interleave / decimation. The LF3320 can be cascaded to realize larger matrices.

The Matrix-vector Multiplication Mode is valid in the Double Wide Data / Coefficient Mode. However, the LF3320 must be configured for single filter mode only, for a maximum [8x8] matrix. The user must disable cascaded filter mode, accumulator access mode, data reversal, and interleave / decimation.

Data reversal can be disabled by setting bit 6, of Configuration Register 1 (Filter A) and Configuration Register 3 (Filter B), both to 1. The Odd-Tap, interleave mode will need to be disabled. Writing a 0 to bit 0 of Configuration Register 1 and Configuration Register 3 will disable the odd-tap interleave mode for Filter A and Filter B. When data is not being interleaved or decimated, the I / D Register length should be set to a length of one (Table 3 and Table 5 in the LF3320 data sheet). Therefore, writing 040H to Configuration Register 1 and 3 will disable the data reversal and set the corresponding inherent characteristics for the desired matrix function.

The Filter A ALU and Filter B ALU are to be configured for A+B (Table 2 and Table 4 in the LF3320 data sheet); so that condition A+0 is satisfied. To accomplish this, bit 0 is reset to 0, bit 1 is set to 1, and bit 2 is reset to 0. Writing 002H to Configuration Register 0 (Filter A) and Configuration Register 2 (Filter B) will set the corresponding registers to satisfy the A+0 condition.

FIGURE 10. CODE USED TO GENERATE DCT MATRIX

```
/*************** INCLUDE HEADER FILES ***************/
#include <math.h>
#define pi 3.141592654
#define Rows 8
#define Columns 8
/******************* MAIN PROGRAM *******************/
int main(void)
{
int i=0,j=0,k=0;
float R1[Rows][Columns]={0},R2[Rows][Columns]={0};
float DCTMTX[Rows][Columns]={0};
/*************** Generate DCT Matrix ****************/
clrscr();   //.Clear display for DCT Matrix printing
for(i=0;i<Rows;i++)
{
     for(j=0;j<Columns;j++)
     {
       if(i==0) //.Generate First Row of DCT Matrix
       {
         ans = (1/sqrt(Rows));
         for(k=0;k<Rows;k++)
           DCTMTX[i][k] = (ans);
       }
       else  //.Generate Remainder of the DCT Matrix
         DCTMTX[i][j] = (sqrt(2(float)Rows))
           *cos((pi*((2*j)+1)*(i))/(2*Rows));
     }
     printf("%9.5f," DCTMTX[i][j]);   //.Print DCTMTX to display
     fflush(stdout);
}
putchar('\n');
return 0;
}
```

It should be noted, writing Configuration Registers 5, 0, 1, and 4 are required when configuring the LF3320 for a 16-point DCT. Writing to Configuration Registers 5, 0, 1, 2, 3, and 4 are required when an 8-point DCT configuration is desired (see Table A and Table B).

Timing Sequence

The timing diagrams in Figure 12 and Figure 13 assume the Configuration Registers, the coefficient sets, and the first set of data values (data set) have been loaded. Loading input data for an [8x8][8x1] matrix operation requires 9 clock cycles and loading input data for a [16x16][16x1] matrix operation requires 17 clock cycles. When configured for an [8x8][8x1] matrix operation, 8 data values are required for loading. When configured for a [16x16][16x1] matrix operation, 16 data values are required for loading. Each data value is fed through the I / D Registers, using the corresponding input.

Once the final data value, of the data set, has been loaded TXFRA / TXFRB should be brought LOW for one clock cycle to complete the loading. Once this occurs, the data set is then bank loaded into the respective registers ready to begin the matrix-vector multiplication operation. The current data set will not change until TXFRA / TXFRB is brought LOW again. To satisfy the matrix equation (see Figure 9), the current data set is held for the duration of the required matrix dimension while cycling (i.e. addressing) through each coefficient set (CENA / CENB must be held LOW). During this time new data values can be loaded serially, without pausing the input data stream, ready for the next activation of TXFRA / TXFRB. To ensure the correct evaluation of the matrix multiplication equation, it is imperative that the coefficient values are paired with their corresponding data values.

For the [8x8][8x1] matrix-vector configuration (dual filter mode), the first result will appear 19 clock cycles from the first data input, DIN11-0 (Filter A) and RIN11-0 (Filter B); device latency for the first result is 10 clock cylces (10+9 = 19). The result will appear at the corresponding filter

TABLE 7. CONFIGURATION REGISTER 5 – ADDRESS 205H

BITS	FUNCTION	DESCRIPTION
0	Cascade Mode	0 : Last In Line 1 : First or Middle in Line
1	Single/Dual Filter Mode	0 : Single Filter Mode 1 : Dual Filter Mode
2	Filter B Input	0 : RIN_{11-0} 1 : DIN_{11-0}
3	Output Adder Control	0 : Filter A + Filter B 1 : Filter A + Filter B (Filter B Scaled by 2^{-12})
4	Matrix Multiply Mode	0 : Disabled 1 : Enabled
5	Accumulator Access Mode	0 : Disabled 1 : Enabled
11-6	Reserved	Must be set to “0”

TABLE A. CONFIGURATION REGISTER LOADING FORMAT - [8 x 8] DCT

	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Config. Reg. 5	R	R	R	R	R	R	0	1	0	0	1	0
Config. Reg. 4	R	R	R	R	R	R	R	R	R	R	1/0*	1/0*
Config. Reg. 1/3	R	R	R	R	R	1	0	0	0	0	0	0
Config. Reg. 0/2	R	R	R	R	R	R	R	R	R	0	1	0

TABLE B. CONFIGURATION REGISTER LOADING FORMAT - [16 x 16] DCT

	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Config. Reg. 5	R	R	R	R	R	R	0	1	0	0	0	0
Config. Reg. 4	R	R	R	R	R	R	R	R	R	R	1/0*	1/0*
Config. Reg. 1	R	R	R	R	R	1	0	0	0	0	0	0
Config. Reg. 0	R	R	R	R	R	R	R	R	R	0	1	0

R = Reserved. Must be set to “0”.
* Refer to LF3320 Data Sheet; will be determined by application requirement.

output, DOUT15-0 (Filter A) and ROUT3-0 / COUT11-0 (Filter B).

For the [16x16][16x1] matrix-vector configuration (single filter mode), the first result will appear 28 clock cycles from the first data input, DIN11-0; device latency for the first result is 11 clock cycles (11+17 = 28). The result will appear at the corresponding filter output, DOUT15-0.

The total pipeline latency for a complete [8x8][8x1] matrix operation is 26 clock cycles and the total pipeline latency for a complete [16x16][16x1] matrix operation is 43 clock cycles. Therefore, to process a complete DCT, of size N=8, a total of 146 clock cycles are all that is required. Similarly, to process a complete DCT, of size N=16, a total of 566 clock cycles are required.

A key operational feature is the ability of the LF3320 to continuously process data without pausing the input or output data streams. Once the pipeline is full, a valid DCT result can be realized at the output on every clock cycle.

Once again, the timing diagrams (see Figure 12 and Figure 13) will assume the Configuration Registers, the coefficient sets, and the data values have been loaded. The corresponding timing diagram loading sequence for the coefficient banks and Configuration / Control registers are included in the LF3320 data sheets (Figure 11 and Figure 12 respectively, in the LF3320 data sheet).

Further reference to timing diagram loading sequence for the RSL registers are also included in the device data sheet (Figure 15, Figure 14, and Figure 13, in the LF3320 data sheet). The Filter A and Filter B LF Interface™ are used to load data into the Filter A and Filter B Configuration Registers and coefficient banks.

Conclusion

Applications requiring the implementation of DCT Block Transformations will benefit from the employment of the LF3320. The separability of the two-dimensional DCT, into one-dimension for each of the columns and rows, is an important property that provides a means of simplification.

When configured for matrix-vector multiplication, the LF3320 takes advantage of this property. A key operational element is the LF3320's ability to load a new data vector while processing the current vector, without interrupting the input or output data streams.

The LF3320 manages the straightforward, computational complexity of an 8 x 8 or 16 x 16 DCT (FDCT or IDCT) with speed and increased bit precision. At an 83 MHz data and computation rate the LF3320 provides an obvious solution to realizing the DCT computational requirements. Additional controls and functionality of the LF3320 simplifies the overall hardware requirements when performing a DCT Block Transformation.

FIGURE 11. BINARY FRACTIONAL, TWOS COMPLEMENT REPRESENTATION

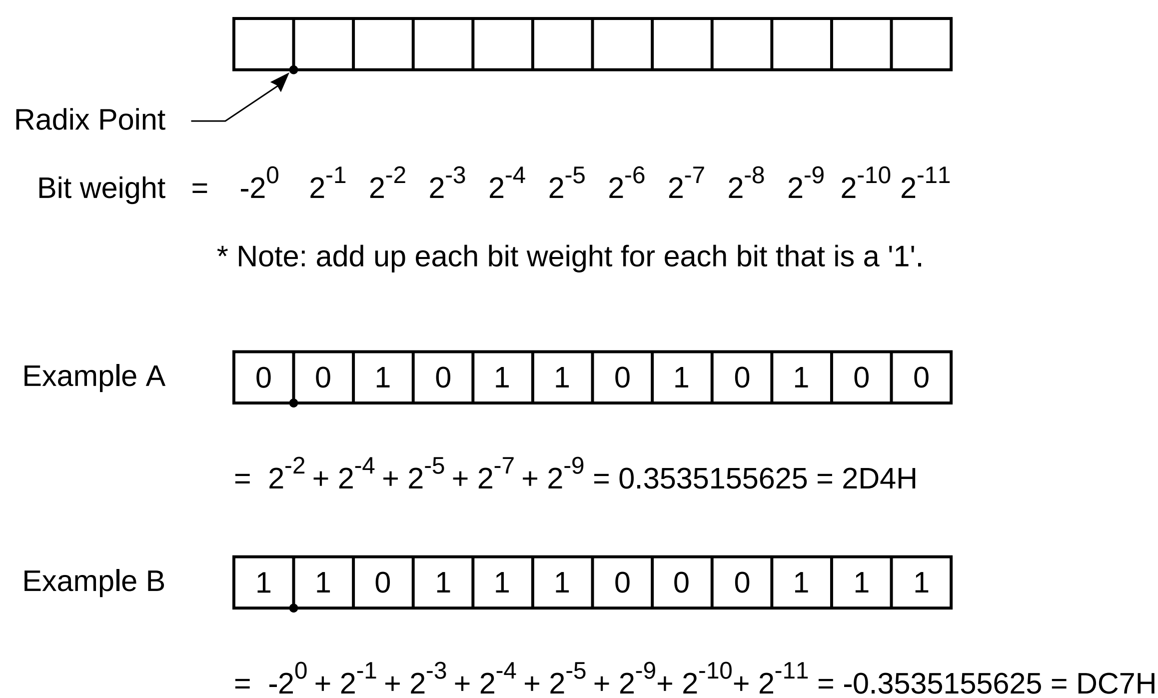
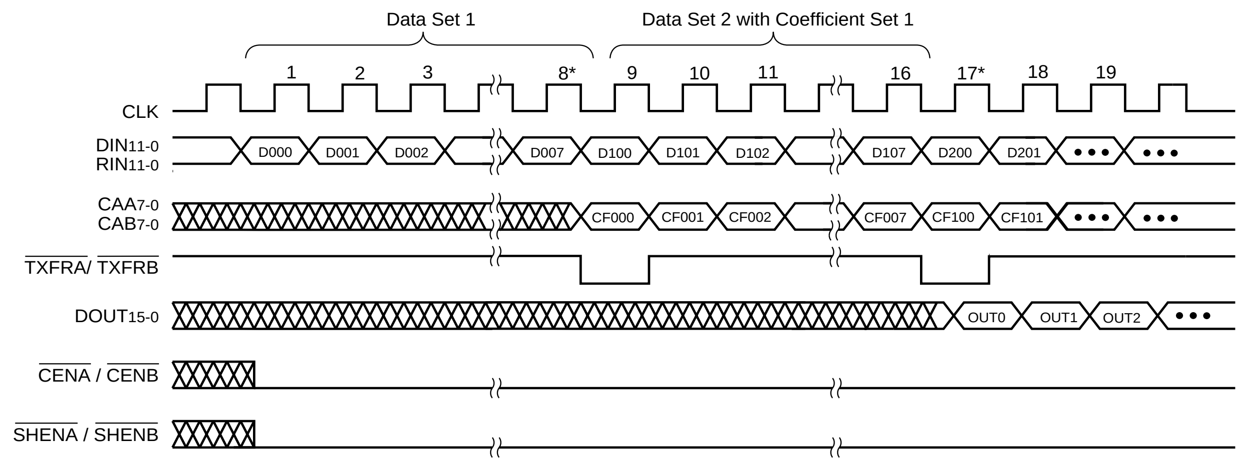
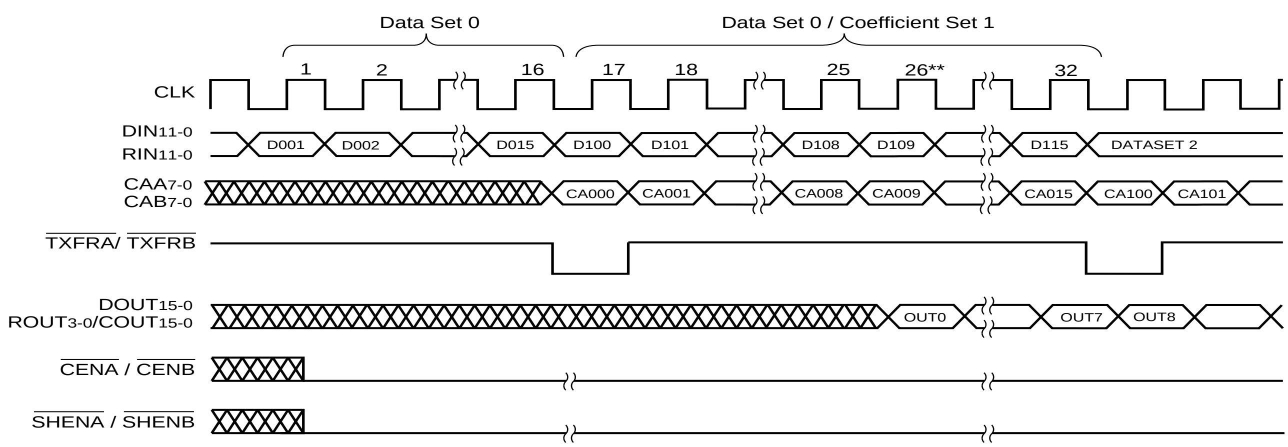


FIGURE 12. DUAL FILTER, MATRIX-VECTOR MULTIPLY TIMING SEQUENCE



*	END of Data Set 1
**	17 Clocks - First Output of First Data/Coefficient Set
***	24 Clocks - Final Output From First Data/Coefficient Set

FIGURE 13. SINGLE FILTER, MATRIX-VECTOR MULTIPLY TIMING SEQUENCE



*	16 Clocks - End of First Data Set
**	26 Clocks - First Output of Data/Coefficient Set 0
	41 Clocks - Final Output of Data/Coefficient Set 0