

## PLD Control of the LF Interface™

### Overview

The Logic Devices LF3300 family of 8 and 12 bit digital filters offer several speed grades including 83MHz, establishing HD video-rate filter solutions for the emerging broadcast and consumer set top box applications. In addition to their video roles, these filters operate in microwave communication receivers and satisfy numerous high-speed digital filter requirements.

Through separate inputs than the data pathway, configuration and control of these devices is achieved with the dual mode LogicFlex, or LF Interface™. The LF Interface™ supports control operations synchronously at the data rate, or from a lower speed, asynchronous controller. This provision of the LF3300 filter family enables the design engineer to choose between targeted system specifications and hardware costs.

Performance and functionality of the filters are maximized when the LF Interface™ is paired with a synchronous interface. In this example, an ASIC is used to initialize filter parameters, sequence the filter control pins, and update coefficients at the system data rate. The LF interface operates with a single load pin,  $\overline{LD}$  and the parallel CF input to configure and load filter coefficients. After setup, operation proceeds with mode control of the filter provided as required, from the ASIC. In FIGURE 1, a coefficient bank load timing diagram, indicates that after the  $\overline{LD}$  pin is lowered, on each rising edge of the CLOCK, a bank address or bank data word is latched until the load sequence is completed. The  $\overline{LD}$  pin is then raised. A 256 coefficient bank, can be updated in 27.7uS, less than the vertical video retrace period. System control and configuration is loaded in this address-data-address-data sequence, similar to the filter coefficients.

When these filters are operated with slower, non-synchronous controllers, a registered type interface must be designed for all inputs and control pins that are synchronously latched by the data CLOCK. CMOS PLD gates are a good choice for this application. These PLD gates are available with low, uniform propagation delays and high clock speeds. Octal latches can be TTL or CMOS PLD gates because these devices must only meet the timing requirements of the slower microprocessor bus.

For the asynchronously controlled filter, the  $\overline{LD}$  pin of the LF Interface™ will operate as described above in the ASIC example. The PAUSE pin is used in conjunction with the LD pin to suspend the data CLOCK to the LF Interface™ for load pacing. With the  $\overline{LD}$  pin held low, the PAUSE must be pulsed low for each address and data word loaded into the LF Interface™. As previously stated, the pulse period must be synchronized to the CLOCK, and each pulse must bracket only one rising edge of the CLOCK. FIGURE 2, shows a coefficient bank load timing diagram, with the  $\overline{LD}$  pin lowered and pulses of the PAUSE pin to latch the CF input data.

Specifically, the microprocessor writes the address word to the CF input and the  $\overline{LD}$  is lowered for one CLOCK. The PAUSE pin must go high after the address word is latched and before the next CLOCK. With the PAUSE pin high, the microprocessor writes the first CF data word. Subsequently, each data word will be written to the CF input and the PAUSE pin pulsed for one CLOCK period. Raising the  $\overline{LD}$  pin after the last data word of the bank registers is latched completes the load cycle. FIGURE 3 is a PLD realization of the control interface for this timing dependency. In this example each time the PAUSE\_IN line is toggled, the PAUSE\_OUT line generates the suitable pulse. FIGURE 4 shows a 12 bit register based on two 74LS374 or PLD374 octal latches for use with 8 bit data buses.

Timing of all control pins except  $\overline{OE}$  must be synchronized to the rising edge of the CLOCK. Therefore, all but this one control pin uses an inverted CLOCK to ensure that logic levels are stable prior to latching. The  $\overline{OE}$  function is latched on the falling CLOCK edge along with the data output and will use a non-inverted CLOCK signal for interface timing. Control pins are categorized in one-of-five groups.

The first group of pins include the CF input used for configuration, control, and data coefficient words, and the  $\overline{LD}$  and PAUSE pins. These are the direct function of the LF Interface™.

The second group is the Round-Select-Limit address pins, the “RSL” used to select the one-of-sixteen output format register sets. These pins select previously registered values for rounding, bit selection, and the clip limit range of the filter output. RSL registers are initially addressed and loaded with the LF Interface™ during filter configuration. Selection of these registers during filter operation is not a LF Interface™ function. A new RSL register set can be selected each CLOCK cycle and the address must be registered externally. A PLD based interface for the RSL address latch is shown in FIGURE 5.

The third pin group controls a previously defined filter configuration to route the data pathways. The transfer pin, TXFR, is used to select the LIFO in data reversal and data set timing for select filter functions. When used, the TXFR control pin is pulsed low for one clock cycle, similar to the operation of PAUSE function.

The shift enable pin,  $\overline{SHEN}$ , is used to enable or disable input data loading into the filter I/D registers and select options for cascade filter modes. The  $\overline{SHEN}$  control pin is pulsed low for one clock cycle, similar to the operation of TXFR and PAUSE pins. As with the second pin group, transfer and shift control are not a function of the LF Interface™. A derivative of the FIGURE 3 PAUSE circuit can be used to generate the TXFR and  $\overline{SHEN}$  pulses, and is shown in FIGURE 6. An external divider may be required to time the period between pulses of the TXFR and  $\overline{SHEN}$  pulse circuit.

The fourth pin group is the data output enable,  $\overline{OE}$ , latched on the falling edge of the CLOCK. The circuit in FIGURE 7 latches the  $\overline{OE}$  signal on the rising edge of the CLOCK.

The fifth pin group includes the CA pins and the CA enable pin,  $\overline{CEN}$ . The CA pins address which filter coefficient bank is selected, and the  $\overline{CEN}$  pin enables the address to be latched. The circuit in FIGURE 6 will generate a single  $\overline{CEN}$  pulse, or instead, use the FIGURE 8 circuit for  $\overline{CEN}$  control. With either circuit, you can use an octal latch to register the bank address, as shown in FIGURE 9. Filter coefficients were loaded through the LF Interface™, however coefficient bank addressing is not a LF function.

## Conclusion

LogicFlex provides a common interface and control mechanism for the Logic Devices video rate digital filter family. Whether your application requires a synchronous controller or the asynchronous microprocessor interface described in this paper, LogicFlex is designed to provide robust filter performance and flexible interface options.

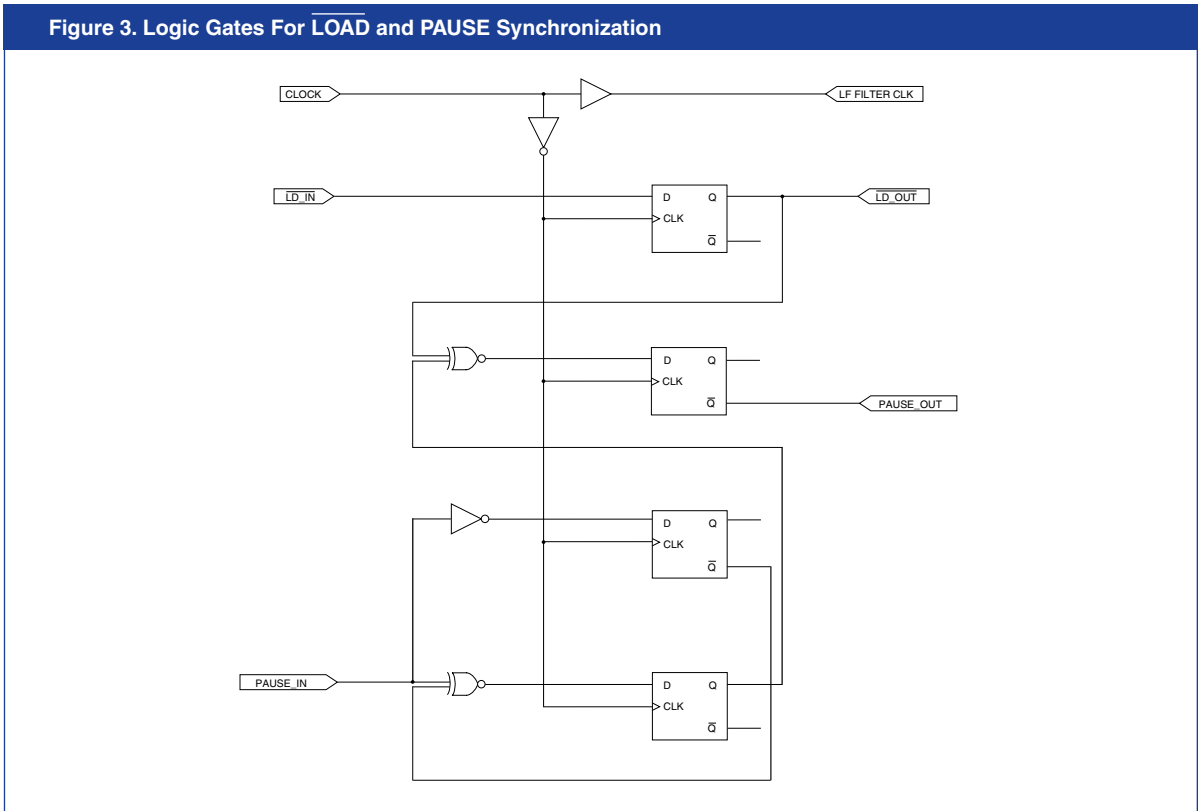
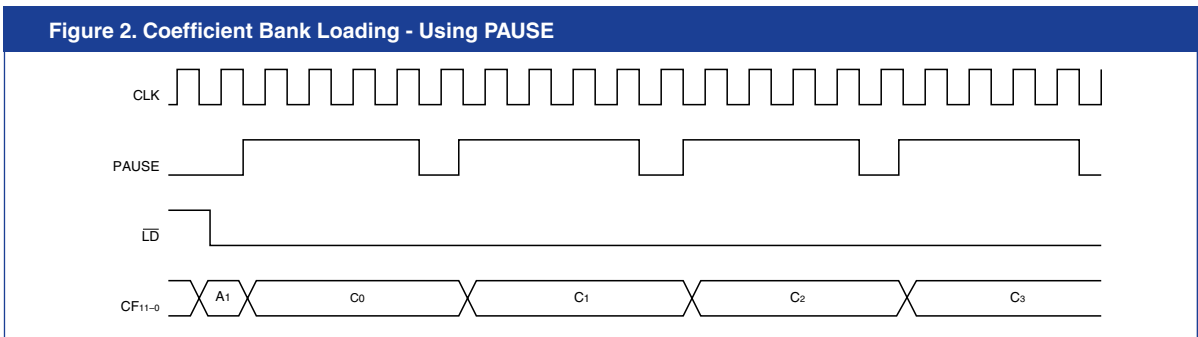
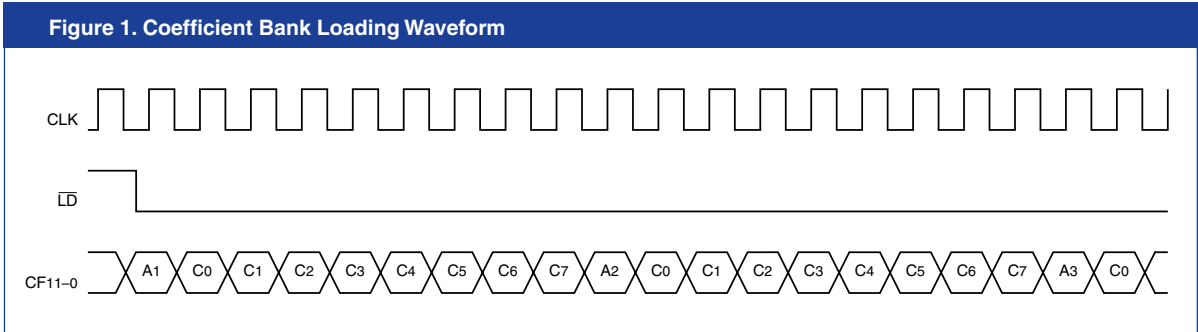


Figure 4. CF Bus Synchronization

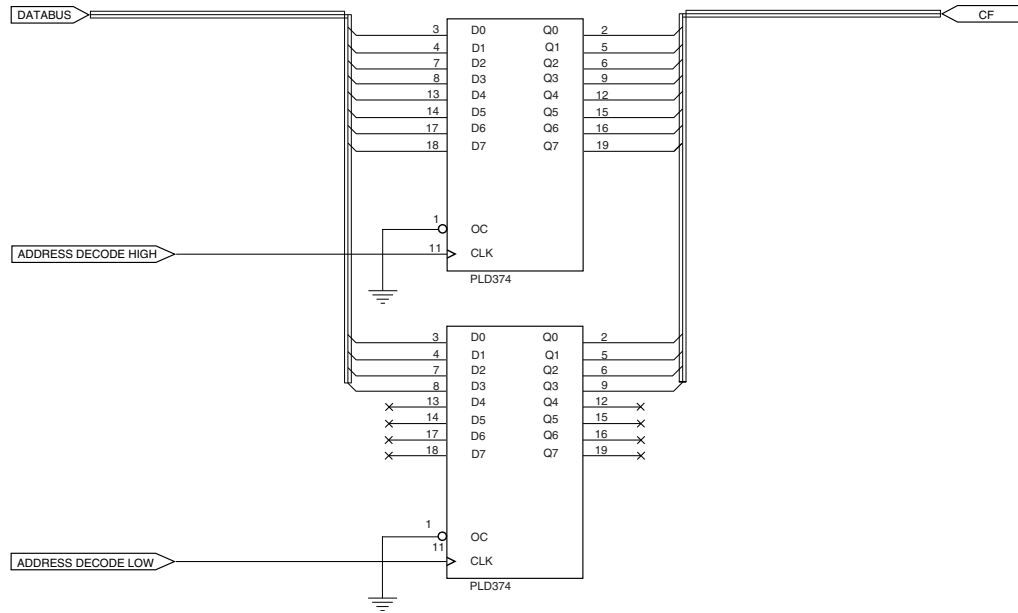


Figure 5. RSL Address Synchronization

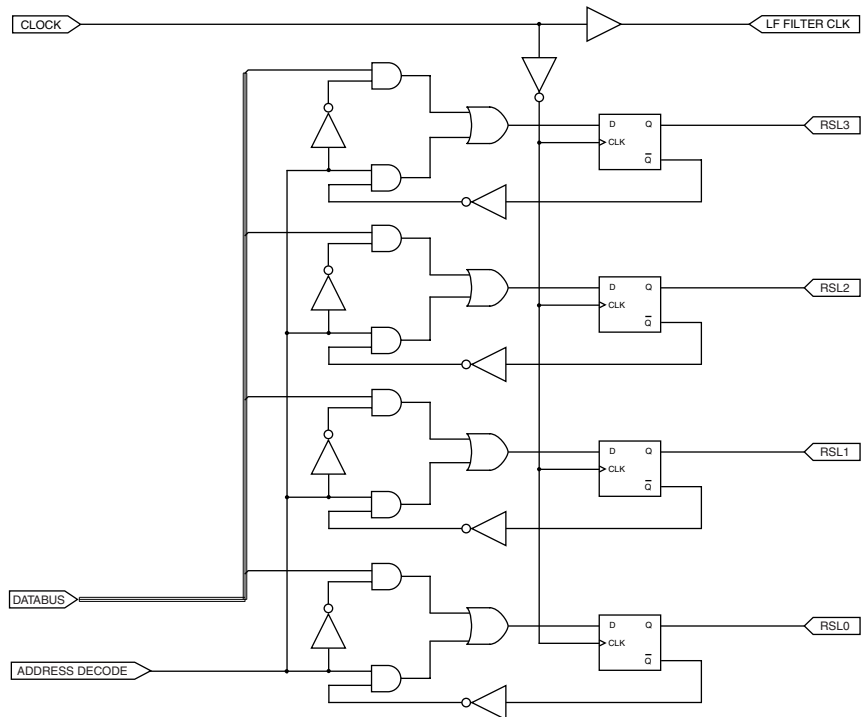


Figure 6. TXFR / SHEN / CEN Pin Synchronization

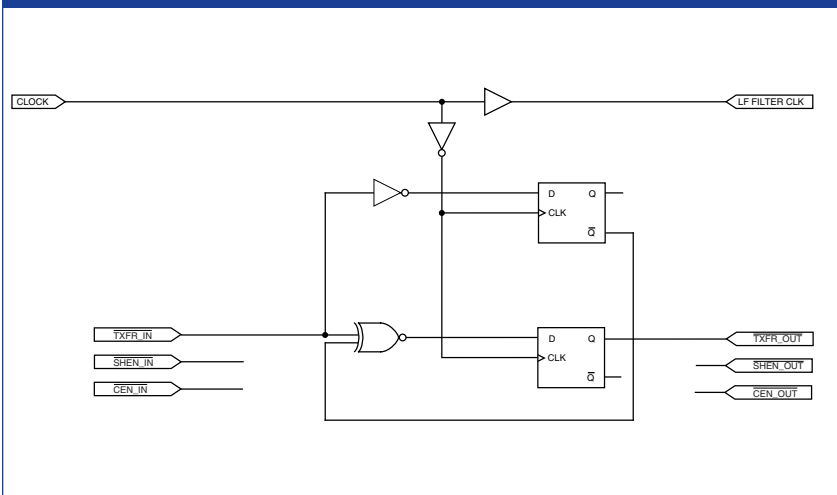


Figure 7. OE Synchronization

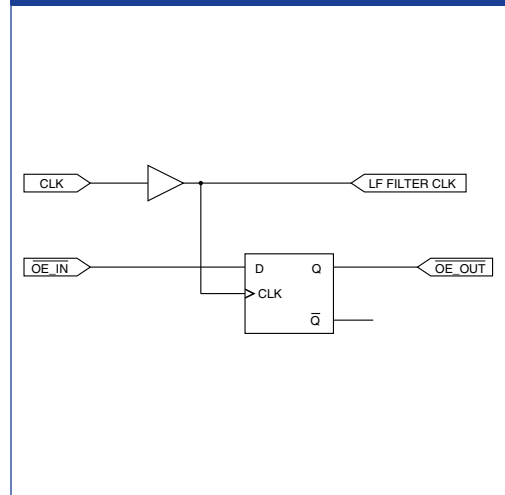


Figure 8. CEN Synchronization

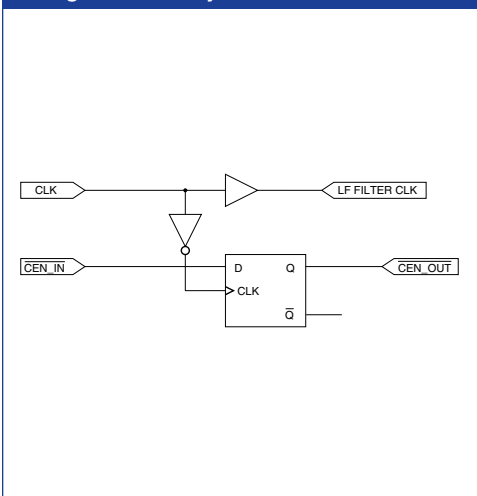


Figure 9. Coefficient Address Synchronization

