

Optimized to support interleaved data sets, the LF3320's architecture provides users with a cost-effective single-chip 32-tap FIR filter while significantly simplifying system design. With a goal of reducing the number of components on a board, the technique of having multiple data sets in a single bit stream (interleaving) is commonly used. To facilitate this, with the aid of the LF3320's Interleave/Decimation Registers (I/D Registers), users can simply program the number of data sets interleaved together and the data is automatically properly aligned (see Interleave/Decimation Registers discussion below).

The LF3320 can handle a maximum of sixteen separate interleaved data sets. Furthermore, with the LF3320's dual filter mode (see Dual Filter Mode discussion below), users may filter up to sixteen data sets interleaved together on both Filter A and Filter B concurrently. To facilitate a unique output control scheme for each interleaved data set, the Rounding/Selecting/Limiting Circuitry (RSL

circuitry) can store sixteen different variations. One important application that will benefit significantly is 4:2:2 filtering where the video signal is already interleaved (see 4:2:2 example below).

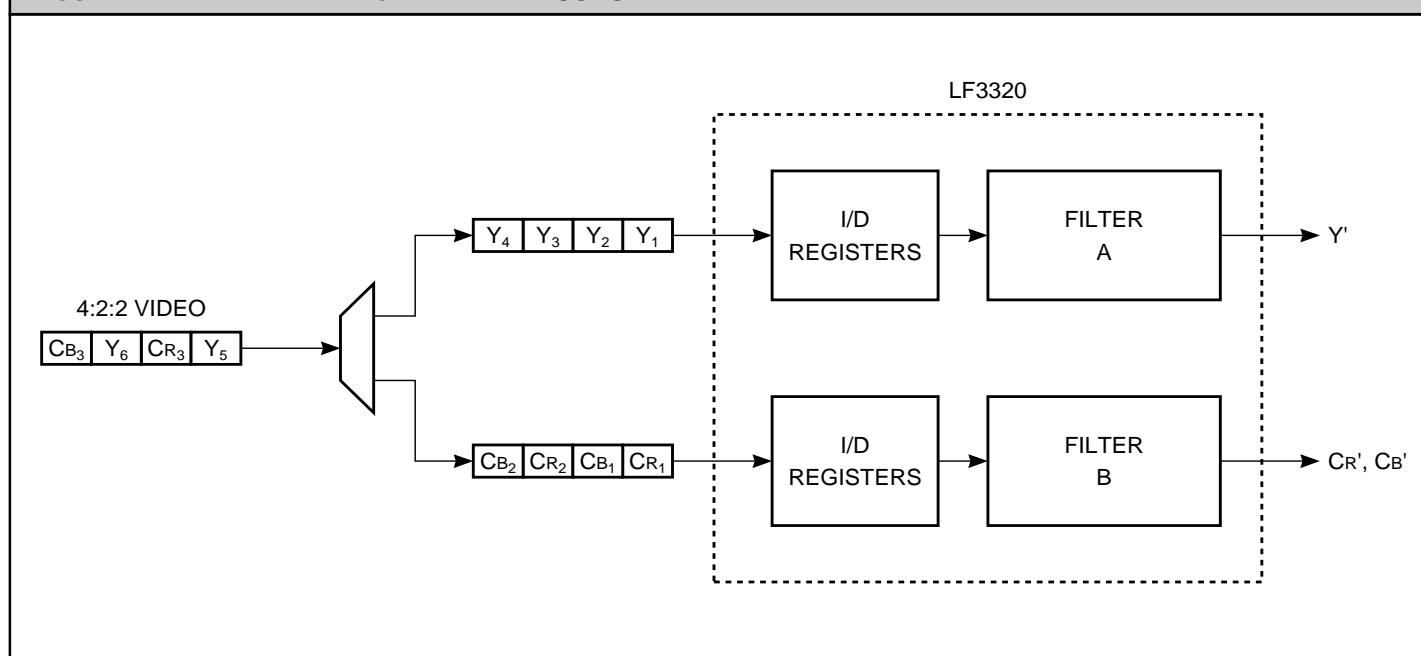
### Interleave/Decimation Registers

The I/D Registers provide the data storage necessary for the device to filter up to sixteen data sets interleaved into the same data stream without having to separate the data sets. The I/D Registers function like variable pipeline registers and can be programmed to have a length from one to sixteen. ALUs placed after the I/D Registers and before the filter taps double the number of filter taps when using symmetric coefficient sets. The ALUs double the number of taps by pre-adding data values prior to multiplication by a common coefficient.

When feeding interleaved data through the device, set the I/D Regis-

ters to a length equal to the number of data sets interleaved together. When non-interleaved data is fed through the device, the I/D Registers should be set to a length of one. Figures 2 and 3 show an example of running two data sets interleaved together through the I/D Registers. The I/D Registers, set to a length of two, accommodate the two data sets. The data path is configured for an odd-tap filter with data reversal disabled. In Figure 2, the I/D Register pipeline is full and data from the first data set appears at the outputs of the I/D Registers. On the next clock cycle, data from the second data set appears at the outputs of the I/D Registers (see Figure 3). Every clock cycle the multipliers filter data from a different data set. Therefore, the coefficients sent to the multipliers should be changed every clock cycle. The LF3320 easily facilitates this by providing a coefficient set address port which determines what coefficient set is used. The address port can be updated every clock cycle allowing the coefficient set to be changed every clock cycle.

**FIGURE 1. 4:2:2 FILTERING WITH THE LF3320**



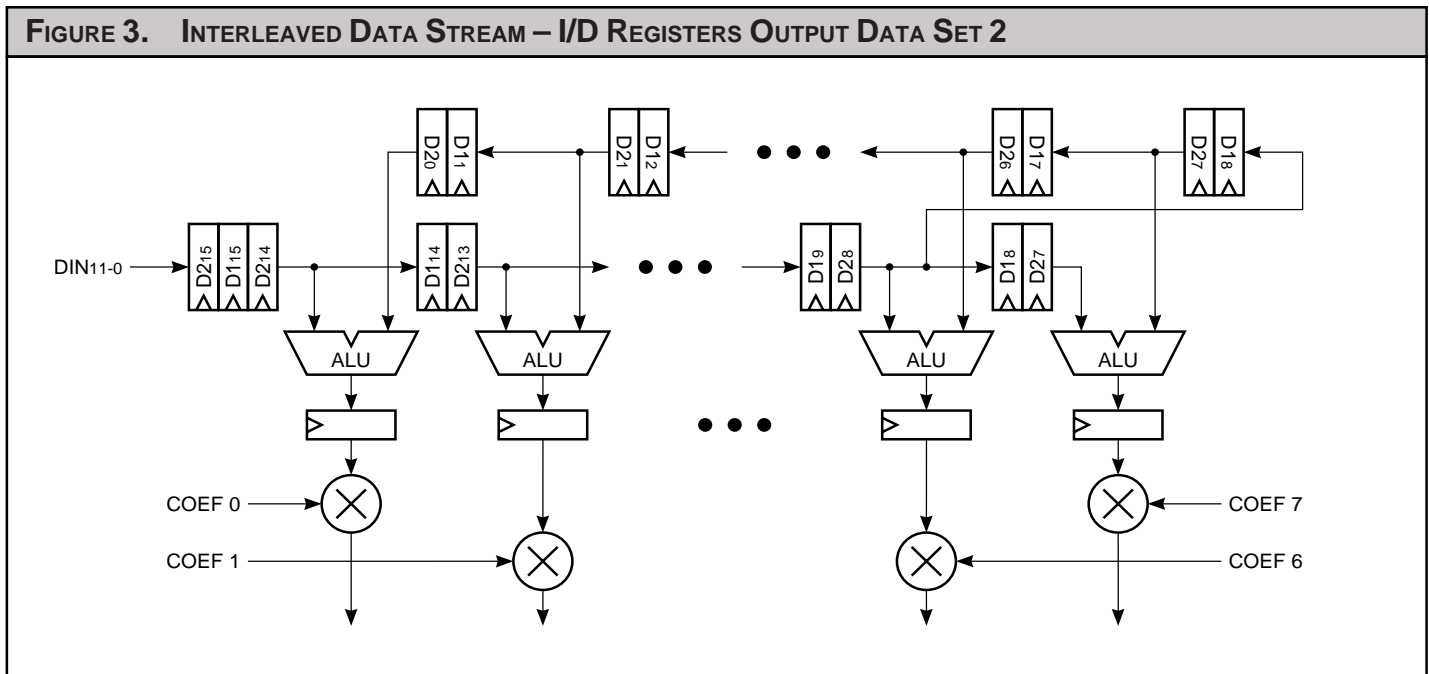
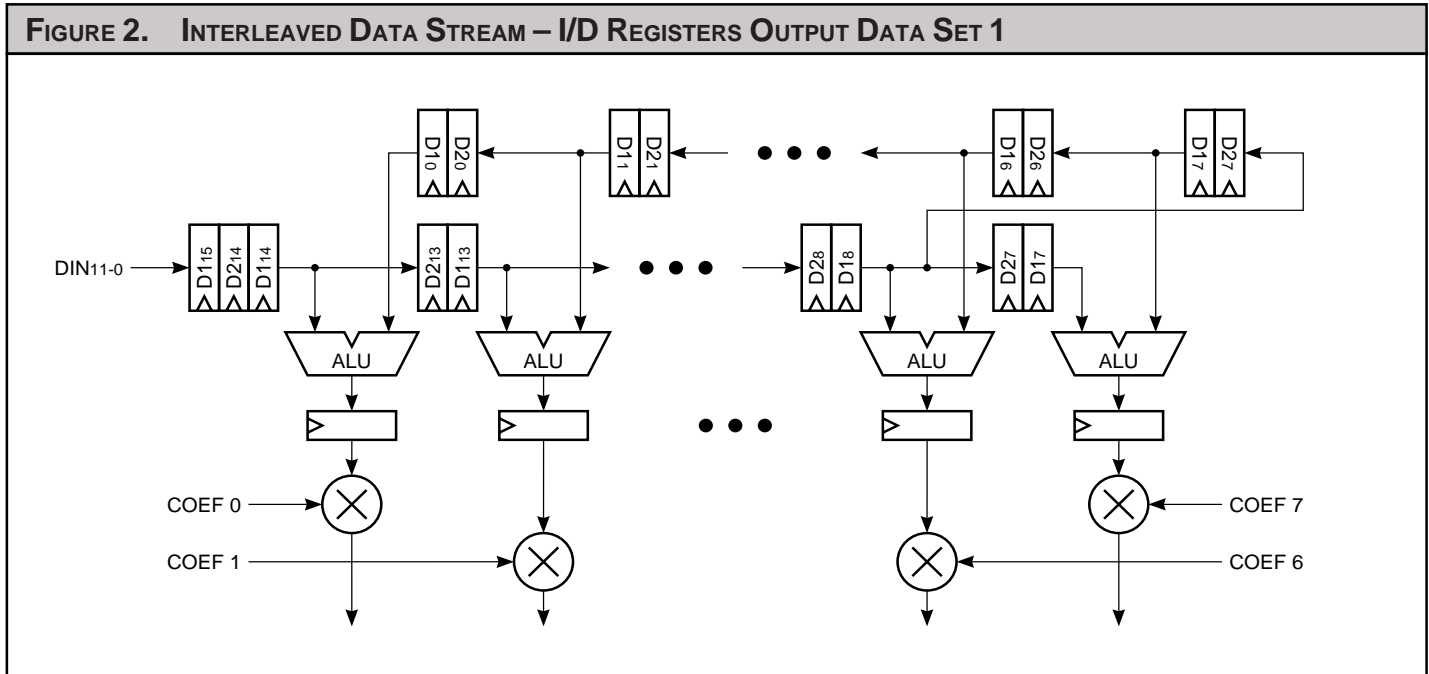
**Dual Filter Mode**

Figure 1 shows the LF3320 when configured for Dual Filter Mode. In this mode, the device operates as two separate FIR filters with a common Master Clock. Each filter can be configured to have as many as sixteen taps if symmetric coefficient sets are used. If asymmetric coefficient sets are

used, each filter can be configured to have as many as eight taps. Outputs for each filter, Filter A and Filter B, are fully pinned out. In addition, there is a fully independent LF Interface™ and RSL Circuitry for each filter side (see LF3320 data sheet for a full discussion on LF Interface™ and RSL Circuitry).

**4:2:2 FILTERING EXAMPLE**

A 4:2:2 video stream consists of three data sets (one luminance and two color difference signals) interleaved together. Three separate filters, one for each data set, are required when filtering 4:2:2 video. Traditionally three separate chips were used but, when using a combination of Dual Filter Mode and Interleaved Mode on the LF3320, 4:2:2 filtering is possible



**TABLE 1. CONFIGURATION REGISTER SETUP FOR 4:2:2 FILTERING**

CONFIGURATION REGISTERS	BIT CONFIGURATION											
	CFA[11]	CFA[10]	CFA[9]	CFA[8]	CFA[7]	CFA[6]	CFA[5]	CFA[4]	CFA[3]	CFA[2]	CFA[1]	CFA[0]
CR0 – 200H	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1
CR1 – 201H	0	0	0	0	0	0/1	0/1	0	0	0	0	0/1
CR2 – 202H	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1
CR3 – 203H	0	0	0	0	0	0	0/1	0	0	1	0	0/1
CR4 – 204H	0	0	0	0	0	0	0	0	0	0	0/1	0/1
CR5 – 205H	0	0	0	0	0	0	0	0	0	0	1	0

on a single chip (see Figure 1). For this example, the luminance signal (Y) is fed into Filter A and the two color difference signals (CR and CB) are fed into Filter B in an interleaved format.

### Device Configuration

Six Configuration Registers are used to configure the LF3320. Configuration Register 5 must be set first. Upon setting Configuration Register 5, the rest of the Configuration Registers (CR0-4) may be set in any order. Table 1 shows the bit configuration for each configuration register and is explained as follows:

#### Configuration Register 5 (205H):

CFA[0] must be set to 0 when in Dual Filter Mode for there is no cascade capability in this mode. CFA[1] is set to 1 to enable Dual Filter Mode. CFA[2] must be set to 0 to select RIN11-0 as the Filter B input port. CFA[3] must be set to 0 when in Dual Filter Mode to bypass the output adder. CFA[11:4] are reserved and must be set to 0.

#### Configuration Register 0 (200H):

CFA[0] is user definable for either odd-symmetric (1) or even-symmetric (0) coefficient sets. CFA[1] and CFA[2] is user definable for either asymmetric or symmetric coefficients. If symmetric coefficient sets are desired, CFA[1] and CFA[2] must be set to 1. If asymmetric coefficient sets are desired, either CFA[1] or CFA[2] must be set to 0

**TABLE 2. CONFIGURATION REGISTER 0 – ADDRESS 200H**

BITS	FUNCTION	DESCRIPTION
0	ALU Mode Filter A	0: A + B 1: B – A
1	Pass A Filter A	0: ALU Input A = 0 1: ALU Input A = Forward Register Path
2	Pass B Filter A	0: ALU Input B = 0 1: ALU Input B = Reverse Register Path
11-3	Reserved	Should be set to “0”

depending on which side of the ALU should be bypassed. CFA[11:3] are reserved and must be set to 0.

#### Configuration Register 1 (201H):

CFA[0] is user definable for enabling Odd-Tap Interleave Mode; this should be disabled if Even-Tap Interleave Mode is desired. The I/D Registers in Filter A are set to a length of one (CFA[4:1] is set to 0000) because the luminance signal is in a non-interleaved format. CFA[5] is user definable for selecting an even (0) or odd (1) number of taps. CFA[6] should be set to 1 to disable Data Reversal. CFA[11:7] are reserved and must be set to 0.

#### Configuration Register 2 (202H):

CFB0 is user definable for either odd-symmetric (1) or even-symmetric (0) coefficient sets. CFA[1] and CFA[2] is user definable for either asymmetric or symmetric coefficients. If symmetric coefficient sets are desired, CFA[1] and CFA[2] must be set to 1. If asymmetric

coefficient sets are desired, either CFA[1] or CFA[2] must be set to 0 depending on which side of the ALU should be set to 0. CFA[11:3] are reserved and must be set to 0.

#### Configuration Register 3 (203H):

CFA[0] is user definable for enabling Odd-Tap Interleave Mode; this should be disabled if Even-Tap Interleave Mode is desired. The I/D Registers in Filter B are set to a length of two (CFA[4:1] is set to 0001) because Filter B is fed two data sets interleaved together. CFA[5] is user definable for selecting an even (0) or odd (1) number of taps. CFA[6] should be set to 1 to disable Data Reversal. CFA[11:7] are reserved and must be set to 0.

**Configuration Register 4 (204H):**  
 CFA[0] is user definable for enabling the limiting function in the Filter B RSL Circuitry. CFA[1] is user definable for enabling the limiting function in the Filter A RSL Circuitry.

**Conclusion**  
 Other devices that facilitate interleaved data sets include the LF3310, LF3330, and LF43168. Other applications for interleaving with this device include RGB filtering, anti-Aliasing, basebanding, etc.

TABLE 3. CONFIGURATION REGISTER 1 – ADDRESS 201H		
BITS	FUNCTION	DESCRIPTION
0	Filter A Odd-Tap Interleave Mode	0: Odd-Tap Interleave Mode Disabled 1: Odd-Tap Interleave Mode Enabled
4-1	Filter A I/D Register Length	0000 : 1 Register 0001 : 2 Registers 0010 : 3 Registers 0011 : 4 Registers 0100 : 5 Registers 0101 : 6 Registers 0110 : 7 Registers 0111 : 8 Registers 1000 : 9 Registers 1001 : 10 Registers 1010 : 11 Registers 1011 : 12 Registers 1100 : 13 Registers 1101 : 14 Registers 1110 : 15 Registers 1111 : 16 Registers
5	Filter A Tap Number	0: Even Number of Taps 1: Odd Number of Taps
6	Filter A Data Reversal	0: Data Reversal Enabled 1: Data Reversal Disabled
11-7	Reserved	Should be set to "0"

TABLE 4. CONFIGURATION REGISTER 2 – ADDRESS 202H		
BITS	FUNCTION	DESCRIPTION
0	ALU Mode Filter B	0: A + B 1: B – A
1	Pass A Filter B	0: ALU Input A = 0 1: ALU Input A = Forward Register Path
2	Pass B Filter B	0: ALU Input B = 0 1: ALU Input B = Reverse Register Path
11-3	Reserved	Must be set to "0"

TABLE 5. CONFIGURATION REGISTER 3 – ADDRESS 203H		
BITS	FUNCTION	DESCRIPTION
0	Filter B Odd-Tap Interleave Mode	0: Odd-Tap Interleave Mode Disabled 1: Odd-Tap Interleave Mode Enabled
4-1	Filter B I/D Register Length	0000 : 1 Register 0001 : 2 Registers 0010 : 3 Registers 0011 : 4 Registers 0100 : 5 Registers 0101 : 6 Registers 0110 : 7 Registers 0111 : 8 Registers 1000 : 9 Registers 1001 : 10 Registers 1010 : 11 Registers 1011 : 12 Registers 1100 : 13 Registers 1101 : 14 Registers 1110 : 15 Registers 1111 : 16 Registers
5	Filter B Tap Number	0: Even Number of Taps 1: Odd Number of Taps
6	Filter B Data Reversal	0: Data Reversal Enabled 1: Data Reversal Disabled
11-7	Reserved	Must be set to “0”

TABLE 6. CONFIGURATION REGISTER 4 – ADDRESS 204H		
BITS	FUNCTION	DESCRIPTION
0	Filter B Limit Enable	0: Limiting Disabled 1: Limiting Enabled
1	Filter A Limit Enable	0: Limiting Disabled 1: Limiting Enabled
11-2	Reserved	Must be set to “0”

TABLE 7. CONFIGURATION REGISTER 5 – ADDRESS 205H		
BITS	FUNCTION	DESCRIPTION
0	Cascade Mode	0: Last In Line 1: First or Middle in Line
1	Single/Dual Filter Mode	0: Single Filter Mode 1: Dual Filter Mode
2	Filter B Input	0: RIN <sub>11-0</sub> 1: DIN <sub>11-0</sub>
3	Output Adder Control	0: Filter A + Filter B 1: Filter A + Filter B (Filter B Scaled by 2 <sup>-12</sup> )
4	Matrix Multiply Mode	0: Disabled 1: Enabled
5	Accumulator Access Mode	0: Disabled 1: Enabled
11-6	Reserved	Must be set to “0”