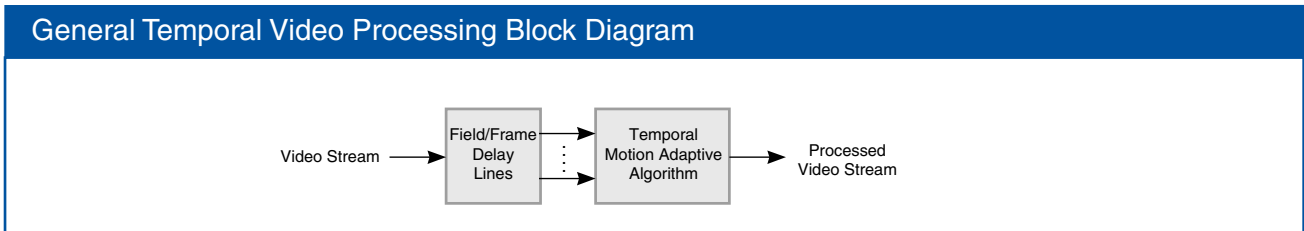




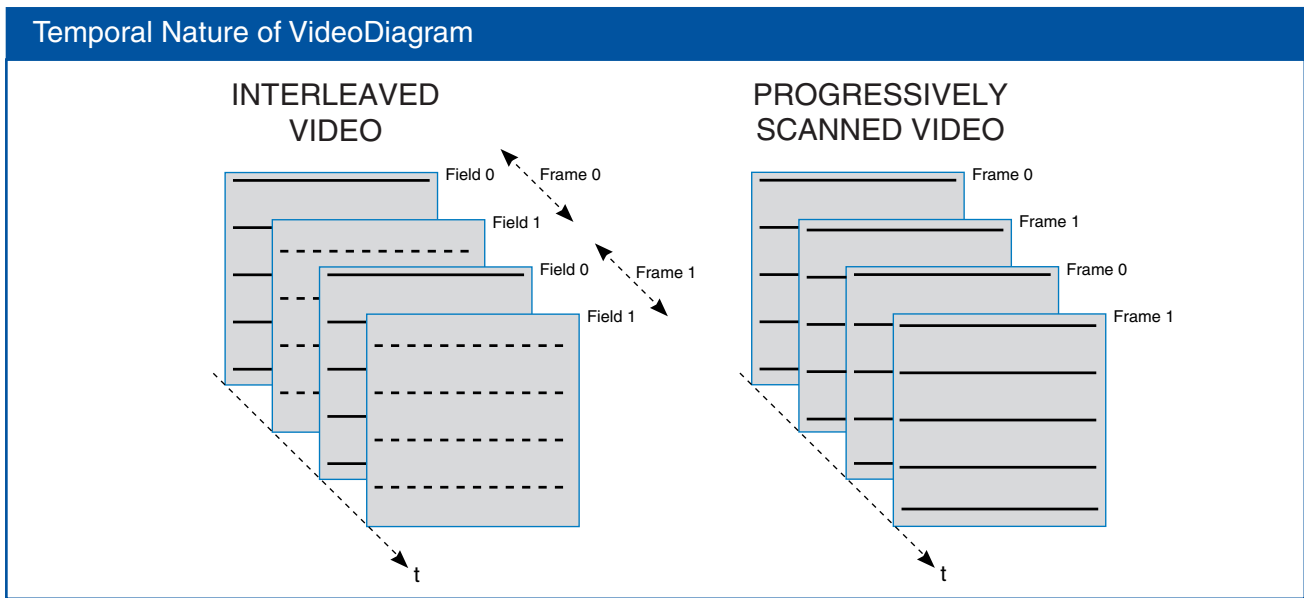
**Overview**

A number of temporal image processing algorithms require field or frame delays in order to gain access to pixels across various points in time. In some instances, wavelet domain denoising in the spatial domain creates artefacts from frame to frame causing unpleasant “flickering” effects. Temporal filtering can suppress the residual artefacts.

In the most general case, a temporal video processing block diagram can be viewed in the following manner:



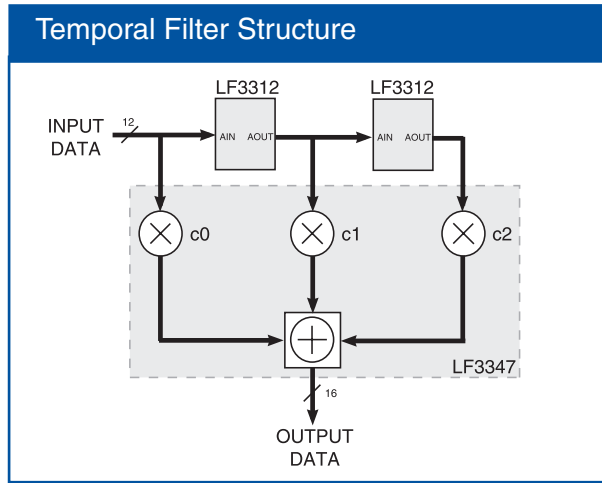
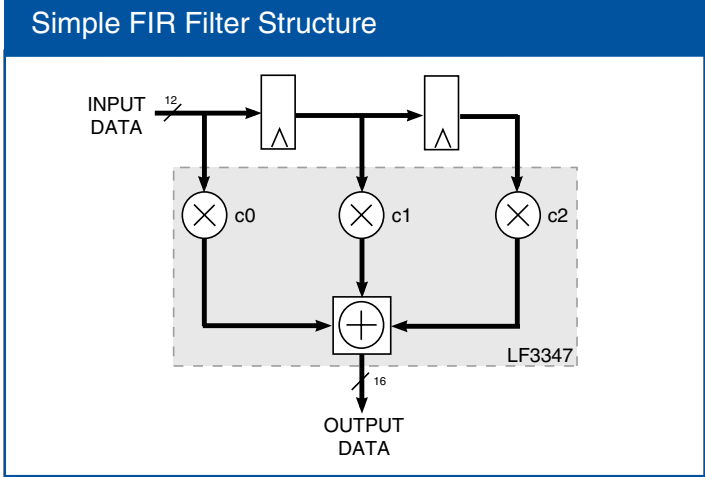
Similar to 1-D FIR filtering, feed-forward temporal (3D) filtering makes decisions on what the current output/sample/pixel/region-of-interest should be, based on present and past inputs. (We will not focus on feedback systems where previous outputs feed back into the decision making process) The following illustrates the temporal nature of frames / fields of video.





Consider the following simple FIR filter block diagram using one of LOGIC Devices DSP Multiply-Accumulate (MAC) building blocks. Simple cycle/sample delay lines are used to space the sequence of inputs. In these simple filters, current outputs are a weighted sum of current and past samples. Filter coefficients are the weights. In simple filters, coefficients are static and normally pre-computed and stored in the hardware. In more complex filters, coefficients/weights can be adaptive and updated on the fly, based on some input/output monitoring processes.

Taken a step further, the 1D filter can be transformed into a 3D filter through the use of field/frame delay lines as illustrated below.



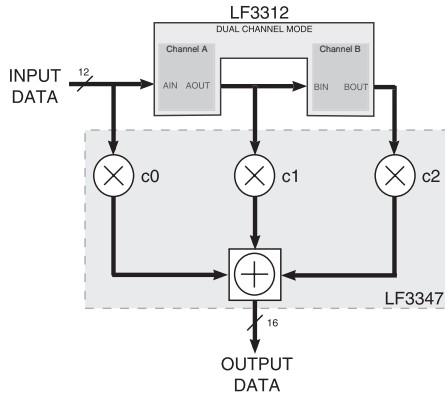
In this 3-tap system, the LF3312 field/frame buffers are used to buffer a complete frame of video, thus allowing the filter to access samples that are a full frame or field apart. Each LF3312 is configured as a synchronous shift register - an extremely deep shift register. The LF3347 implements the "mixer", which weights and sums a pixel's present and past values. It supports 12bit input data and 12bit coefficients and runs at a maximum clock frequency of 83MHz. The sum is internally rounded and limited/clamped based on user programmable parameters.

The LF3312 can be configured as two 6Mbit memories with dual independent read/write ports (dual-channel mode). If a field/frame can be accommodated in 6Mbits, the delay lines of a 3-tap 3D filter can be implemented in a single LF3312 device. The following per-channel depths are available in dual-channel mode:

- 777,600 samples deep x 8 bit words (per channel)
- 622,080 samples deep x 10 bit words (per channel)
- 518,400 samples deep x 12 bit words (per channel)



#### Single-Device - Two Field/Frame Delays



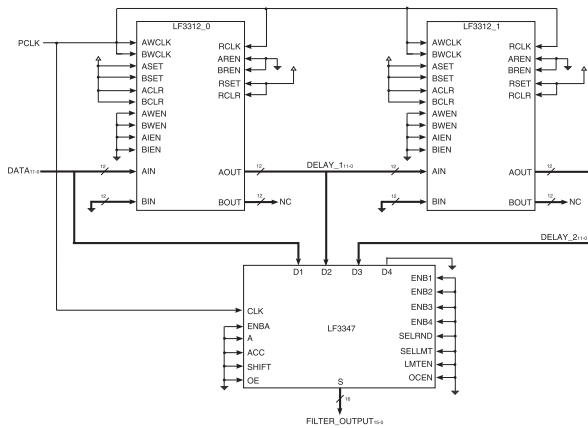
The block diagram to the left illustrates the LFI3312 performing two delay lines in a single device:

The rest of the document is dedicated to the general schematics of implementing the LFI3312 and LFI3347 in the two configurations described above.

**NOTES:**

- Please reference the LFI3312 appnote entitled "Frame Delay in Shift Register Mode" to get specific configuration details.
- Please reference the LFI3347 datasheet in order to better understand the Multiply Accumulate device.

#### Filter using Frame Delays - LFI3312 Single Channel



#### Filter using Frame Delays - LFI3312 Dual Channel

