

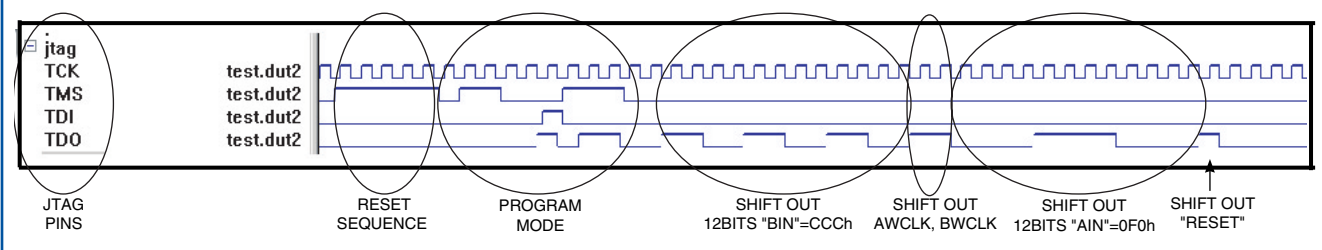


## Overview

Upon validating a new design, the first step is often verifying IC pin/ball connections. This app brief discusses using JTAG boundary scan to capture pin connection information, with a specific focus on the I2C pins.

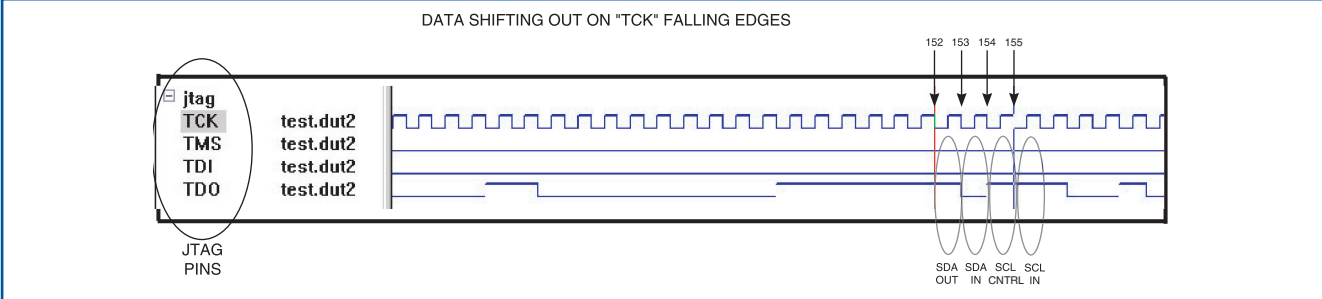
The following waveform illustrates the use of the JTAG interface bits to get into the Sample/Preload instruction mode. A Reset cycle begins the sequence by leaving TMS HIGH for 5 rising edges of TCK. Sample/Preload is selected by loading the 2-bit "01"

### Sample/Preload Waveform



In the BSDL file, one can see that the SDA/SCL pins are scan chain registers 152 through 155. That is, these captured scan register bits appear on TDO after 152 falling edges of TCK. Since SDA is a bidirectional port, the scan chain offers both SDA-OUT (the signal the device is driving onto the SDA pin) and SDA-IN (the input signal that the device captures on the SDA pin). The SCL port is an input whose capture register is 155. The SCL pin is input-only, yet its scan cell still has an output signal (register 154) that is internally tied HIGH.

### Shift Out Captured Scan Register Bits



The following behavioural Verilog code resets the Tap controller, runs through the SAMPLE/PRELOAD process, resets the controller again, and finally runs the EXTEST instruction. The Sample/Preload instruction performs two functions. First, it captures the status of all of the device pins, and shifts them out of the TDO port. Second, it allows the user to shift test bits into the scan registers, on TDI, in order to later force them onto the pins. The EXTEST instruction, once initiated, forces the previously shifted-in bits onto the pins. This instruction also captures input pin data bits. In the Sample/Preload sequence of the following, the TDI port is tied LOW for simplicity. It effectively shifts zeros into all of the scan chain registers. The last bit of the EXTEST sequence puts the Tap controller into the "update IR" state on the rising edge of TCK. On the subsequent falling edge of TCK the output pins are forced into the states determined by preloaded scan chain bits.



### Example Verilog code for JTAG Control and Communication

```

//*****
// reset sequence
    for (cnt=0; cnt < 5; cnt=cnt+1)
        begin
            #(tcr) tms=1; tdi=0; // goto test logic reset
        end
//*****
// sample/preload bit1=0 bit0=1 [01] ---- just capture and shift
#(tcr) tms=0; tdi=0; // goto run_test/idle
#(tcr) tms=1; tdi=0; // goto select dr scan
#(tcr) tms=1; tdi=0; // goto select ir scan
#(tcr) tms=0; tdi=0; // goto capture ir
#(tcr) tms=0; tdi=0; // goto shift ir
#(tcr) tms=0; tdi=1; // goto shift ir    bit 0
#(tcr) tms=1; tdi=0; // goto exit 1    bit 1
#(tcr) tms=1; tdi=0; // goto update ir
#(tcr) tms=1; tdi=0; // goto select dr scan
#(tcr) tms=0; tdi=0; // goto capture dr
    for (cnt=0; cnt < 165; cnt=cnt+1)
        begin
            #(tcr) tms=0; tdi=0; // goto shift dr falling edge bit 'cnt'
        end
//*****
// reset sequence
    for (cnt=0; cnt < 5; cnt=cnt+1)
        begin
            #(tcr) tms=1; tdi=0; // goto test logic reset
        end
//*****
// extest bit1=0 bit0=0 [00] ---- just capture and shift
#(tcr) tms=0; tdi=0; // goto run_test/idle
#(tcr) tms=1; tdi=0; // goto select dr scan
#(tcr) tms=1; tdi=0; // goto select ir scan
#(tcr) tms=0; tdi=0; // goto capture ir
#(tcr) tms=0; tdi=0; // goto shift ir
#(tcr) tms=0; tdi=0; // goto shift ir    bit 0
#(tcr) tms=1; tdi=0; // goto exit 1    bit 1
#(tcr) tms=1; tdi=0; // goto update ir
//*****
// reset sequence
    for (cnt=0; cnt < 5; cnt=cnt+1)
        begin
            #(tcr) tms=1; tdi=0; // goto test logic reset
        end
//*****
    
```