

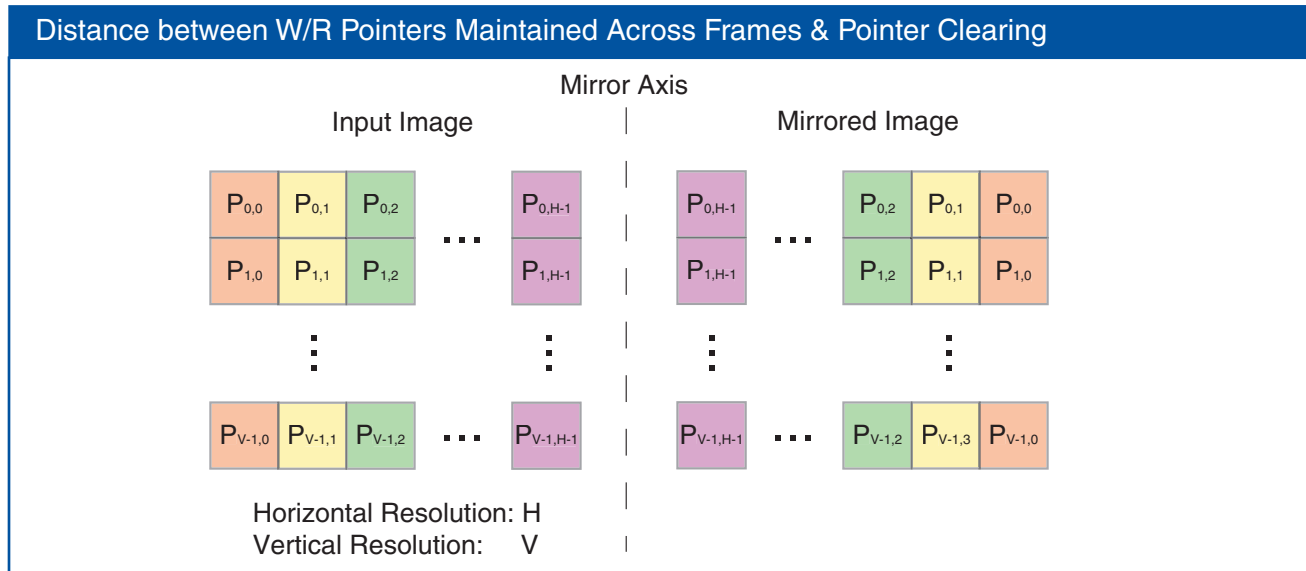


## Overview

With the LF3312's flexible memory address architecture, data can be sequentially stored in memory and then accessed using a completely reordered address. An application such as creating the 'mirror image' of a frame of video is a good example of this addressing flexibility.

The memory would accept the pixel data as typical raster scanned video.

$P_{0,0} P_{0,1} P_{0,2} \dots P_{0,H-1} P_{1,0} P_{1,1} P_{1,2} \dots$



Through real-time address manipulation we can easily rearrange the order we read the stored data - resulting in the 'mirror image' of the frame of video. The common raster scan method starts at the first line, scans left to right and then increments the line address. We can also start from the first line, but instead scan from right to left and then increment the line address.

The resulting pixel order would look like

$P_{0,H-1} P_{0,H-2} \dots P_{0,0} P_{1,H-1} P_{1,H-2} \dots$

## Address Manipulation

For this particular application, just over one line of video needs to be stored. A spacing of at least one line of video between the write and read addresses must be maintained. Reading a line in the reordered sequence can only begin after a full line has been written.

The input pixel data will be automatically written into memory as sequential data. That is, the write address is incremented sequentially like a FIFO with no external addressing needed.

The read address reordering however does require the use of external addressing on every read cycle. The LF3312 offers a 24bit external address port for applications such as this that require Random Access addressing. Of course, not all of the 24bits of address need to be dynamically controlled. Depending on the resolution, much of the MSB address bits can be tied off and ignored.

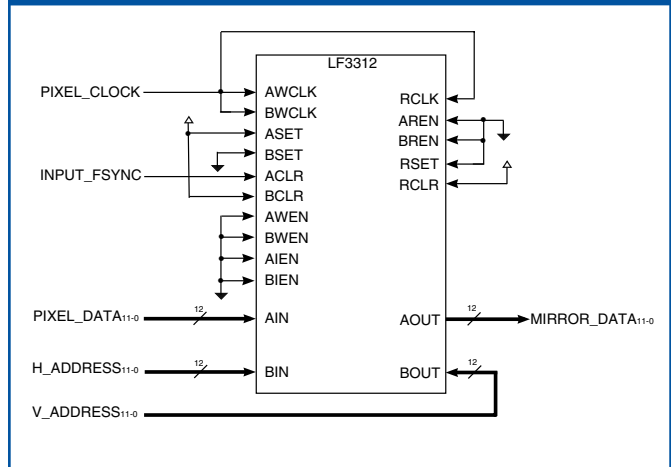
For image manipulation applications, the LF3312 is capable of internally remapping its internal linear address space into a X/Y Cartesian coordinate system. We can access image data in terms of line/column or horizontal/vertical addresses. This greatly simplifies the address controller.

### Implementation Details

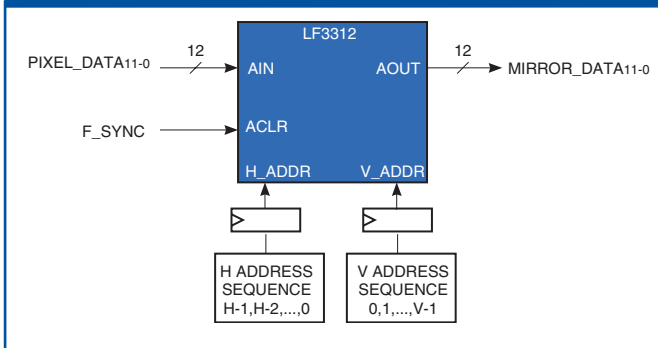
The LF3312 must be placed in single channel random access mode (Register 8[2:0] = 001). Single channel allows us to use the full depth of the memory and it allows us to cascade devices for greater depth, and it frees up the BIN/BOUT ports - which act as the 24bit external address port. The Random Access mode invalidates any empty/full FIFO considerations and allows us to manipulate the write/read pointers as we wish.

In for the device to remap a Horizontal/Vertical address into a linear address, the horizontal resolution (line-length) must be provided. This is programmed using the 16bit ROWLENGTH control register (Registers 0 & 1). For example, for a line-length of 1280 pixels, we would load ROWLENGTH as 500hex.

### Pin Connection Diagram



### Pin Connection Diagram



The BIN port is used as the Horizontal address and the BOUT port is the Vertical address. The Cartesian coordinates are internally mapped to the memory's linear address space as:

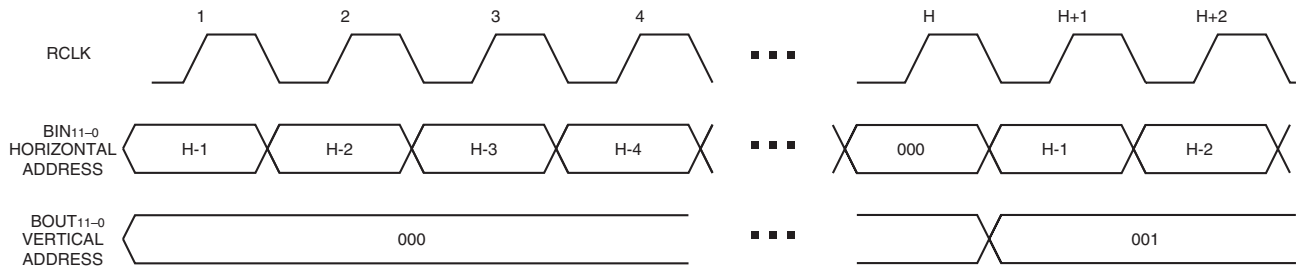
$$\text{Internal memory address} = (\text{BOUT} \times \text{ROWLENGTH}) + \text{BIN}$$

In order to select the external BIN/BOUT 24bit address port as the source of the Read-address, BSET=0 and BCLR=1. Bringing RSET LOW forces the read-address to this external address. RSET can be programmed to be level or negative edge triggered. In order to continuously force the read pointer to an external address, RSET must be programmed to be level sensitive - and kept LOW.

An external frame-sync signal must reset the write pointer at the start of every input frame. This maintains the address reference (the first pixel of Line 0 is always defined as address 0). The ACLR pin resets the write pointer when brought LOW. NOTE: ACLR can be programmed to be level or negative edge triggered.

**HD FRAME MEMORY**

Re-ordering of the Read Address to Implement a "Mirror Image" Effect



- \* Rising edges 1 through H latch the address of the pixels of Line 0 in reverse order.
- \* Rising edges H+1 through 2H repeats the Horizontal reordering of Line 1, and so-on.
- \* The contents of memory addresses supplied by BIN/BOUT appear on the AOUT port 14 rising edges of RCLK after the address is latched.

