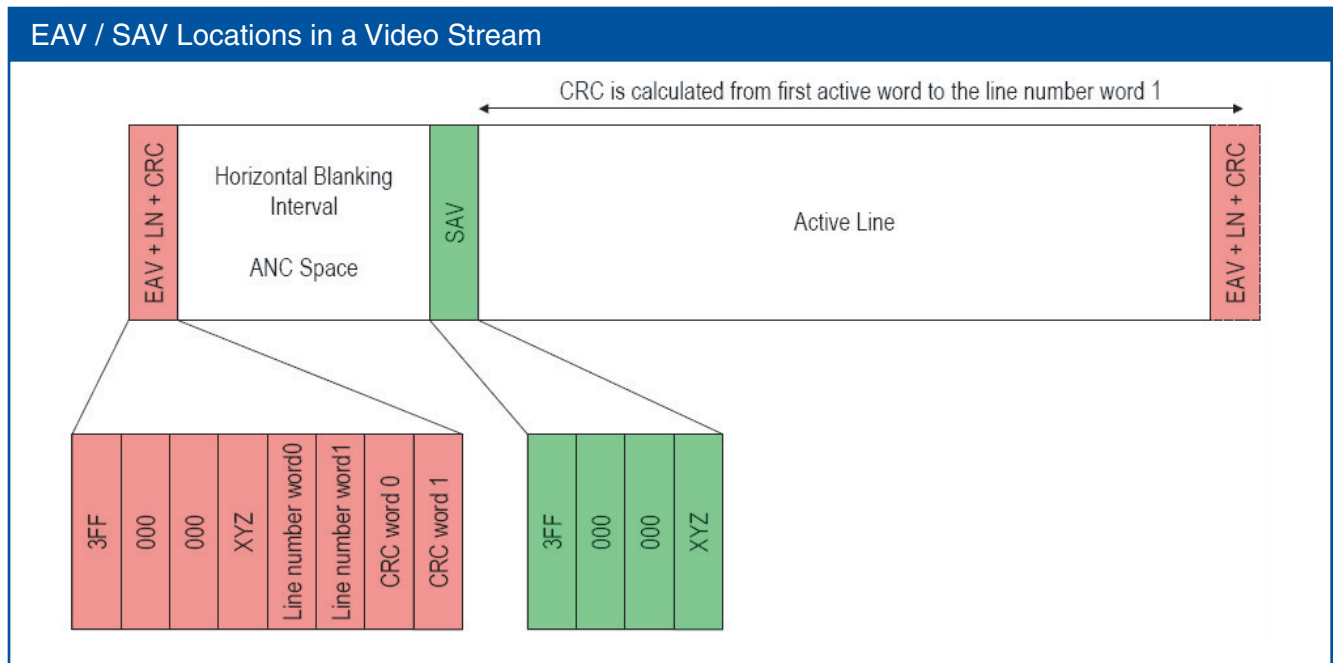




Overview

Timing Reference Signals (TRS) embedded in video streams. These ‘markers’ embedded in the data define active video and blanking intervals as seen in the figure below. TRS words come in two flavors: End of Active Video (EAV) and Start of Active Video (SAV). The EAV/SAV sequence is different depending on the field (Odd/Even) or blanking interval (H-blanking and/or V-blanking). In video synchronization and manipulation applications, the field (F-bit) is of particular interest. Using this F-bit, the Video Memory can determine the beginning of a field or frame and react to it by setting or clearing the Write pointer. By monitoring the F-bit within EAV/SAV sequences, the Write pointer can be set, cleared, or marked. In addition to manipulating the write pointer, the embedded F, V, and H bits from the input data can be output on the external Flag pins in various combinations.



Using Embedded TRS Words to Clear the Write Pointer

When using the TRS data, the LF3312 should be placed in one of the two FIFO modes: single-channel FIFO mode (Register 8[2:0]=011) or dual-channel FIFO mode (Register 8[2:0]=111)

The ‘F’ bit within embedded TRS video data can be used to RESET the Write pointer on frame or field boundaries (Register 9 [7:5]=110 resets pointer on frame boundaries, Register 9 [7:5]=111 resets pointer on field boundaries). For frame-based resets, the Write pointer is reset by the EAV that exhibits an F bit that is LOW, where the previous EAV exhibited an F bit that was HIGH. This EAV sequence is saved in its entirety in the first 4 locations of memory; addresses 0, 1, 2, and 3.

In order to trigger the memory to reading the frame/field of video just written to memory, starting from address 0, we must issue an RCLR signal. Upon bringing RCLR LOW (again, this read pointer reset can be level or edge triggered), the Read pointer is reset. In all FIFO modes, it takes 9 AREN-enabled rising edges of RCLK for the contents of address 0 to arrive on AOUT when an RCLR is issued.



Using Embedded TRS Words to Set/Jump the Write Pointer

The 'F' bit within embedded TRS video data can also be used to SET the Write pointer (Register 9 [7:5]=100 sets pointer on frame boundaries, Register 9 [7:5]=101 sets pointer on field boundaries). For frame-based sets, the Write pointer can be set by the EAV that exhibits an F bit that is LOW, where the previous EAV exhibited an F bit that was HIGH. This EAV sequence is saved in its entirety beginning with address N. Address N can come from the pre-loaded ALAT register (using Registers 2,3, & 4 - and setting BSET LOW) or from the BIN/BOUT ports (setting BSETB HIGH).

In order to trigger the memory into reading the frame/field of video just written to memory, starting from address N, we must issue an RSET signal. Upon bringing RSET LOW (again, this read pointer reset can be level or edge triggered), the Read pointer is set to predefined address N. Again, address N can come from the pre-loaded BLAT register (using Registers 5,6, & 7 - and setting BSET LOW and BCLR LOW) or from the BIN/BOUT ports (setting BSET LOW and BCLR HIGH). In all modes, it takes 14 AREN-enabled rising edges of RCLK (including the edge to latch a LOW on RSET) for the contents of address N to arrive on AOUT when a RSET is issued.

Displaying Out-bound TRS bits on Output Flags

TRS timing bits can be displayed on the A and/or B flag output pins. The F, V, and H bits can be extracted directly from the input data stream or from the buffered output data stream.

When the LF3312 is in a single channel mode, Register B[3:0] controls which TRS bits are mapped to which output flag pin. In dual channel modes, Register B[3:0] controls Channel A's TRS bit mapping, and Register B[7:4] controls Channel B TRS bit mapping.

4TH Word of the EAV / SAV Code (passed to AIN[11:0] or BIN[11:0])												
Word Width	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8 bit	1	F	V	H	X	X	X	X	----	----	----	----
10 bit	1	F	V	H	X	X	X	X	X	X	----	----
12 bit	1	F	V	H	X	X	X	X	X	X	X	X

Frame Based Video Synchronization using Embedded TRS Words

The LF3312 in single-channel FIFO mode can synchronize incoming frames within a video stream to a Master/Local frame sync signal. Address zero within the memory is the reference for the start of frame. The Write and Read clocks should be tied to the incoming pixel clock and outbound master/system clock respectively. The embedded TRS data in the video clears the Write pointer on frame boundaries (on every falling edge of F-bit). In addition to synchronizing the data, the LF3312 can display the TRS F, V, and H bits from the synchronized video on the APE, APF, and ACOLLIDE pins respectively for monitoring purposes or for timing reference further down the data path.

The only control pin that requires management is the RCLR pin, which should be tied to a system/master F-sync signal. Bringing RCLR LOW requests a new frame using the system/master clock domain. It takes 9 AREN-enabled rising edges of RCLK for the contents of address 0 to arrive on AOUT, the first sample of the new frame. The RCLR "frame/field sync" timing should be referenced to RCLK, the system/master video clock.