

OVERVIEW

Cascading multiple LF3312s for depth expansion is easy. The usable 24bit address space is simply extended for every additional device that is cascaded.

The LF3312 is cascaded in parallel, where the input of each device is tied together. The input data word (the data word placed on the AIN input port) is to be common for all devices. Similarly, the outputs of all devices are tied together. Only one device drives the shared output bus at one time, controlled automatically through internal bus enables.

During operation, each device's write and read pointers are identical. Each device in a cascade of N devices is responsible for 1/N of the address space. That is, each device writes and/or reads based on the common W/R pointer locations and where that particular device sits in the cascade. Configuration Register C[3:0] (BASE_ADDR) is used to define each device's place in the cascade.

For example, in 10bit mode, each LF3312 has 1,244,160 address locations (0 to 12FBFF). When the cascade's common write pointer is between address 0 and 12FBFF, the device with BASE_ADDR=0 actively writes into its memory. When the common write pointer either advances, or is SET to an address in the 12FC00 to 25F7FF region, the device with BASE_ADDR=1 actively writes into its memory. Reading from memory works in the same fashion.

When cascading LF3312s, only single-channel modes are supported (OPMODES 0 to 3). All write enables AWEN/BWEN and AIEN/BIEN must be tied together, as must read enables AREN/BREN (see the device connection diagram on the next page).

The configuration registers of each device must be programmed identically, depending on mode/function, except for Register C. Register C defines which region of the 24bit address space the particular device is responsible for. Within Register C, there is a 4bit BASE_ADDR and 4bit CASCADE word. BASE_ADDR determines the region of address space each device controls, and CASCADE defines how many devices are in cascade.

Example) 3 devices cascaded. Each device's Register C programmed as the following:

CHIP 0

Configuration Register Address	Data[7:0]	Description
C	02	Chip 0 out of 3 devices in cascade

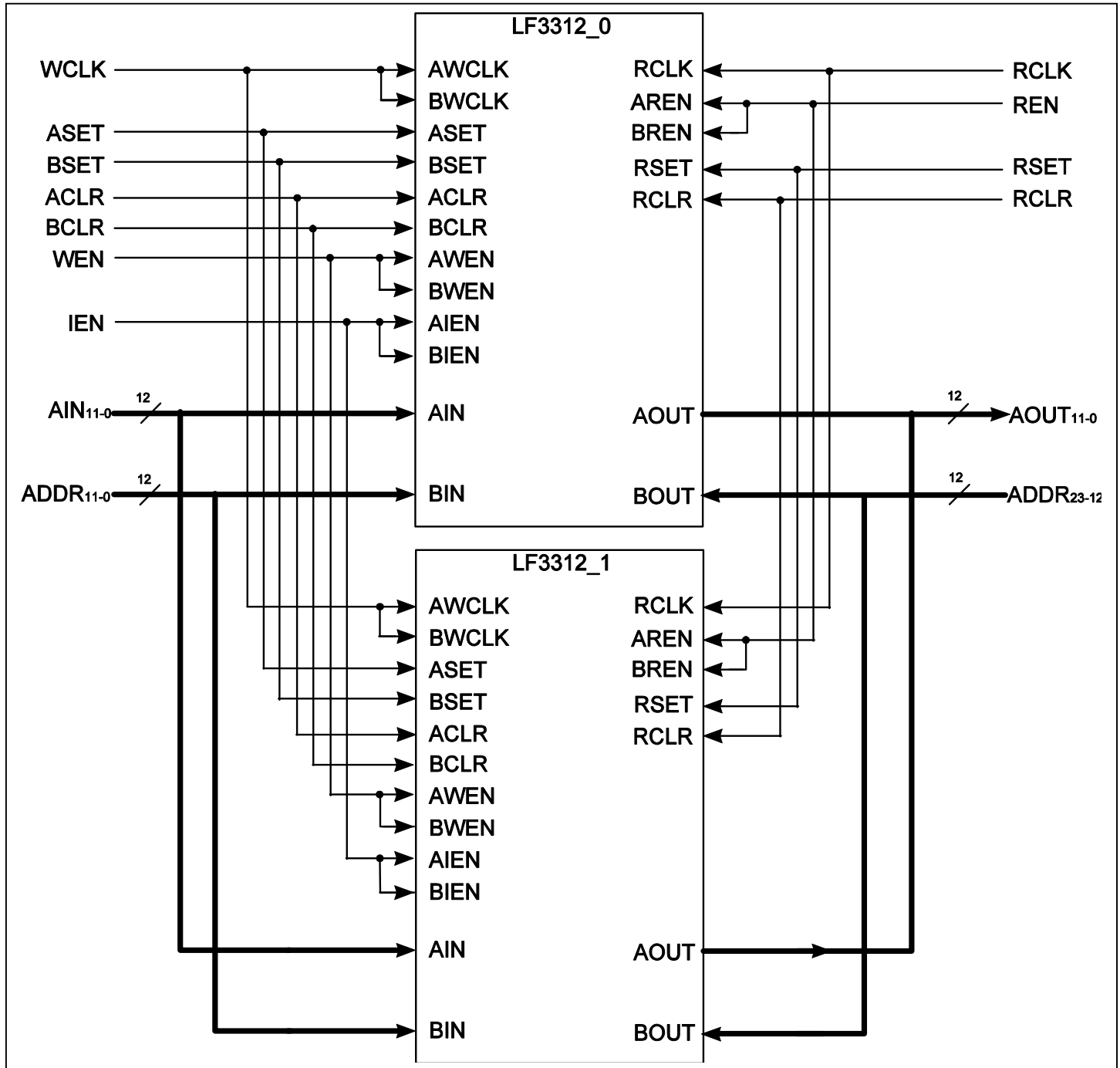
CHIP 1

Configuration Register Address	Data[7:0]	Description
C	12	Chip 1 out of 3 devices in cascade

CHIP 2

Configuration Register Address	Data[7:0]	Description
C	22	Chip 2 out of 3 devices in cascade

Device Connection: Two Cascaded LF3312s - General Purpose Connection



NOTE: The above diagram connects two cascaded LF3312s in the most general-purpose case. Here, all pointer-control pins are accessible for manipulating the pointers. If your application does not require a particular control pin, it can simply be tied off. All additional cascaded devices should be connected to 'LF3312_0' as 'LF3312_1' does.