

This application brief describes the LF3312’s programmable flag behaviour. The first section describes the Empty/Full threshold settings. The second section provides a simple example of how the flags react to enabled writes and reads to/from the memory.

PROGRAMMABLE EMPTY THRESHOLDS

The APE / BPE flags are HIGH when the WRITE pointer is ahead of the READ pointer by less than or equal to a certain number “X” of address locations or Clock cycles.

```
IF (W_address – R_address) ≤ X ,
    APE=HIGH
ELSE
    APE = LOW
```

The following tables outline the specific number “X” of locations or clock cycles for the various programmable ‘Threshold’ levels in both Single-Channel and Dual-Channel modes.

“X” values for Single Channel Mode

Empty Threshold	Data Width		
	8 bit	10 bit	12 bit
1/80	19,214	15,371	12,809
2/80	38,414	30,731	25,609
3/80	57,614	46,091	38,409
4/80	76,814	61,451	51,209
5/80	96,014	76,811	64,009
6/80	115,214	92,171	76,809
7/80	134,414	107,531	89,609
8/80	153,614	122,891	102,409

“X” values for Dual Channel Mode

Empty Threshold	Data Width		
	8 bit	10 bit	12 bit
1/80	9,614	7,691	6,409
2/80	19,214	15,371	12,809
3/80	28,814	23,051	19,209
4/80	38,414	30,731	25,609
5/80	48,014	38,411	32,009
6/80	57,614	46,091	38,409
7/80	67,214	53,771	44,809
8/80	76,814	61,451	51,209

PROGRAMMABLE FULL THRESHOLDS

The APF / BPF flags are HIGH when the WRITE pointer is ahead of the READ pointer by greater than a certain number “Y” of address locations or Clock cycles.

```
IF (W_address – R_address) > Y ,
    APF=HIGH
ELSE
    APF = LOW
```

The following tables outline the specific number “Y” of locations or clock cycles for the various programmable ‘Threshold’ levels in both Single-Channel and Dual-Channel modes.

“Y” values for Single Channel Mode

Full Threshold	Data Width		
	8 bit	10 bit	12 bit
79/80	1,535,999	1,228,799	1,023,999
78/80	1,516,799	1,213,439	1,011,199
77/80	1,497,599	1,198,079	998,399
76/80	1,478,399	1,182,719	985,599
75/80	1,459,199	1,167,359	972,799
74/80	1,439,999	1,151,999	959,999
73/80	1,420,799	1,136,639	947,199
72/80	1,401,599	1,121,279	934,399

“Y” values for Dual Channel Mode

Full Threshold	Data Width		
	8 bit	10 bit	12 bit
79/80	767,999	614,399	511,999
78/80	758,399	606,719	505,599
77/80	748,799	599,039	499,199
76/80	739,199	591,359	492,799
75/80	729,599	583,679	486,399
74/80	719,999	575,999	479,999
73/80	710,399	568,319	473,599
72/80	700,799	560,639	467,199

FIFO CONTROLS WHEN USING EMPTY/FULL FLAGS

In FIFO applications using the programmable empty/full flags, the Writes and Reads to/from the memory should be controlled by the write enable (AWEN) and read enable (AREN) respectively. During a burst of writing, AWEN should be LOW, and when the burst of writing has stopped AWEN should be brought back HIGH. The same is true for bursts of reading. NOTE: clearing the write or read pointers invalidates the empty/full flags.

SIMPLE EXAMPLE

Example Situation:

- 10bit Single-Channel mode
- Empty threshold = $2 / 80$, $X = 30,731$
- Full threshold = $78 / 80$, $Y = 1,213,439$

The device is powered up, and a hard or soft master reset (using the RESET) pin is issued. The APE flag is HIGH and the APF flag is LOW. A burst of writing begins, AWEN is brought LOW. After 30,730 write cycles (with no read cycles), the APE flag is still LOW. Upon the 30,731st write cycle, the APE flag is driven LOW on the rising edge of RCLK. The APE flag remains LOW as long as the WRITE pointer is at least 30,731 locations ahead of the READ pointer. Let us assume that no reads have occurred and the write burst continues. After the 1,213,439th write cycle the APF flag is still LOW. On the 1,213,440th write, the APF flag is driven HIGH.