

IEEE 1149.1 Serial Boundary Scan (JTAG)

The LF3312 incorporates a serial boundary scan test access port (TAP) in its BGA package. This device is compliant with IEEE Standard #1149.1-1900.

Test Access Port Clock - TCK

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select - TMS

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a HIGH level when left floating.

Test Data Input - TDI

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP controller state diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data Output - TDO

The TDO pin is used to serially pass data from the internal TAP registers. The output is active depending on the current state of the TAP state machine (see instruction codes). The output is updated on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A TAP reset is performed by forcing TMS HIGH for five consecutive rising edges of TCK. A reset can also be initiated by bringing TRST LOW and issuing a rising edge of TCK. These resets do not affect the operation of the LF3312 and may be performed while the device is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is serially output from the TDO pin on the falling edge of TCK.

Instruction Register

Two-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

Bypass Register

To save time when serially shifting data through registers, it is sometimes required that certain chips be skipped. The bypass register is a single bit register that can be placed between TDI and TDO. This allows data to be shifted through the device with minimum latency. The bypass register is preset LOW when the Bypass instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the I/O pins on the device. The boundary scan register captures the state of these pins when the controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST and SAMPLE/PRELOAD instructions can be used to capture the contents of the input and output 'ring'. The Boundary Scan Order table show the order in which the bits are connected. The MSB of the boundary scan register is connected to TDI, and the LSB of the register is connected to TDO.

Identification Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE instruction has been loaded. The IDCODE is hardwired into the device and can be shifted out onto TDO when the TAP controller is in the Shift-DR state. The ID register has the vendor code and other information described in the Identification Register Definition table.

TAP Instruction Set

Four instructions are possible with the 2-bit instruction register. Combinations are listed in the Instruction Register Definition table. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. To execute the instruction, the TAP controller must pass through the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also placed the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded upon power-up and during resets states.

BYPASS

When the BYPASS instruction is loaded and the TAP controller placed in the Shift-DR state, the bypass register is placed between the TDI and TDO pins. By using BYPASS, the boundary scan path can be shortened when multiple devices are daisy-chained together on a board.

SAMPLE/PRELOAD

The Sample/Preload instruction captures a snapshot of the I/O pins, when in the Capture-DR state.

Since the TAP controller can only operate at a much lower rate than the device clocks, it is possible that during a 'capture' of the I/O states, a signal may undergo a transition. In this case, there is no guarantee which value will be captured. Repeatable results may not be possible.

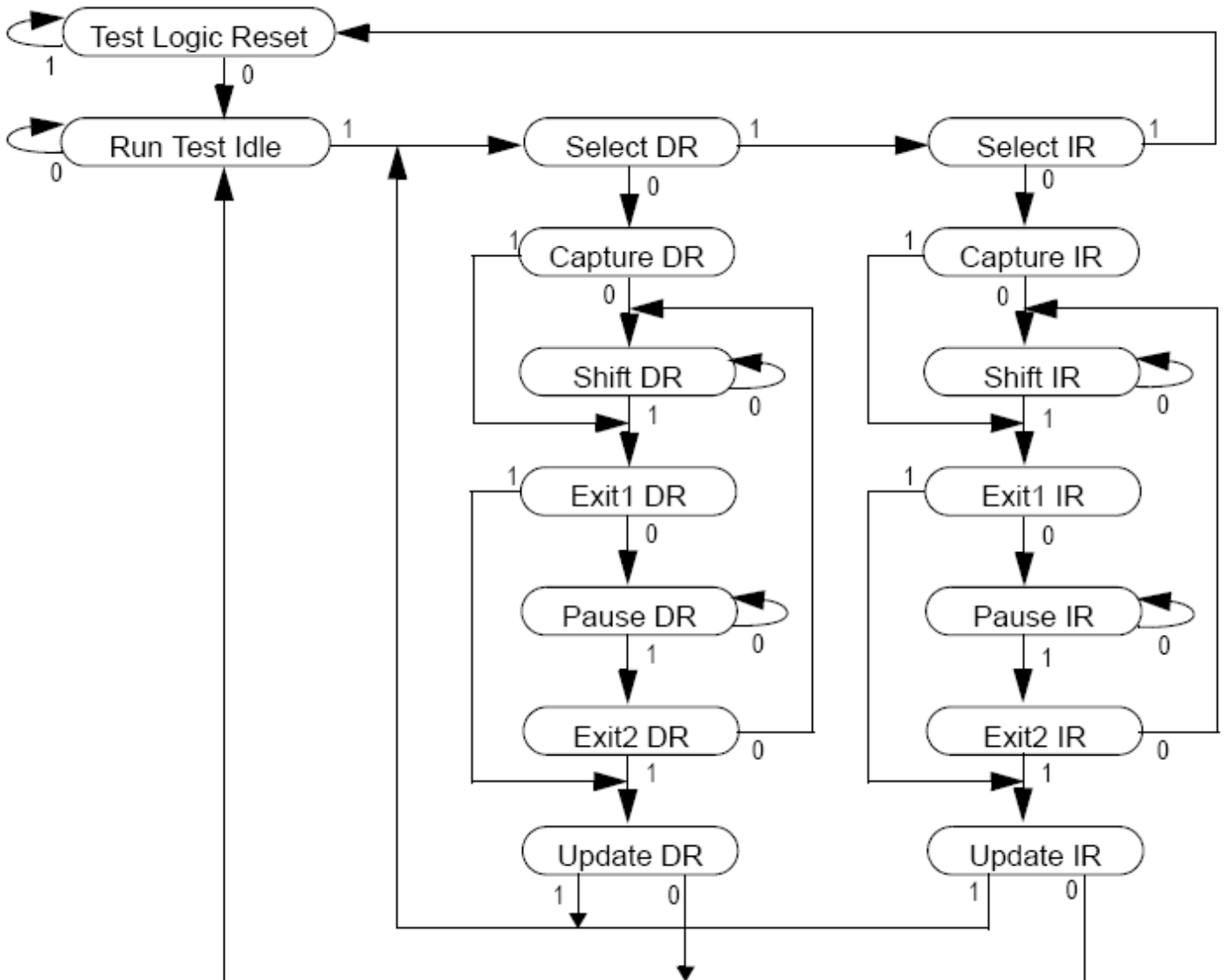
Once data is captured, it is possible to shift out the data by placing the TAP controller in the Shift-DR state, which places the boundary scan register between TDI and TDO.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan test operation (often prior to forcing the output pins to this pattern using the EXTEST instruction). NOTE: while data is captured and shifted out, preloaded data can be shifted in.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. The instruction also selects the boundary scan register to be connected for serial access between TDI and TDO in the Shift-Dr controller state.

TAP Controller State Diagram



Boundary Scan Order

Please see the BSDL file on the LF3312 webpage for boundary scan details.

Identification Register Definition

Identification Field	Value	Description
Revision Number (31:28)	0000	Version number
LOGIC Device ID (27:12)	0011001100010010	Defines device type
LOGIC JEDEC ID (11:1)	01000110010	Unique device vendor ID
ID Register Presence (0)	1	Indicate presence of ID register

Instruction Register Definitions

Bit 1	Bit 0	Instruction	Description
0	0	EXTEST	Forces output states, boundary scan register between TDI & TDO
0	1	Sample/Preload	Captures I/O states, boundary scan register between TDI & TDO
1	0	IDCODE	Loads ID register with ID code, ID register between TDI & TDO
1	1	BYPASS	Places Bypass register between TDI & TDO

JTAG AC Characteristics

Symbol	Parameter	Min	Max	Units
tJCYC	JTAG TCK clock period	100	-	ns
tJCH	JTAG TCK clock HIGH	40	-	ns
tJCL	JTAG TCK clock LOW	40	-	ns
tJS	JTAG input Setup	15	-	Ns
tJH	JTAG input Hold	15	-	ns
tJDH	JTAG Data Output Hold	0	-	ns
tJD	JTAG Data Output Delay	-	25	ns

JTAG Timing Specifications

