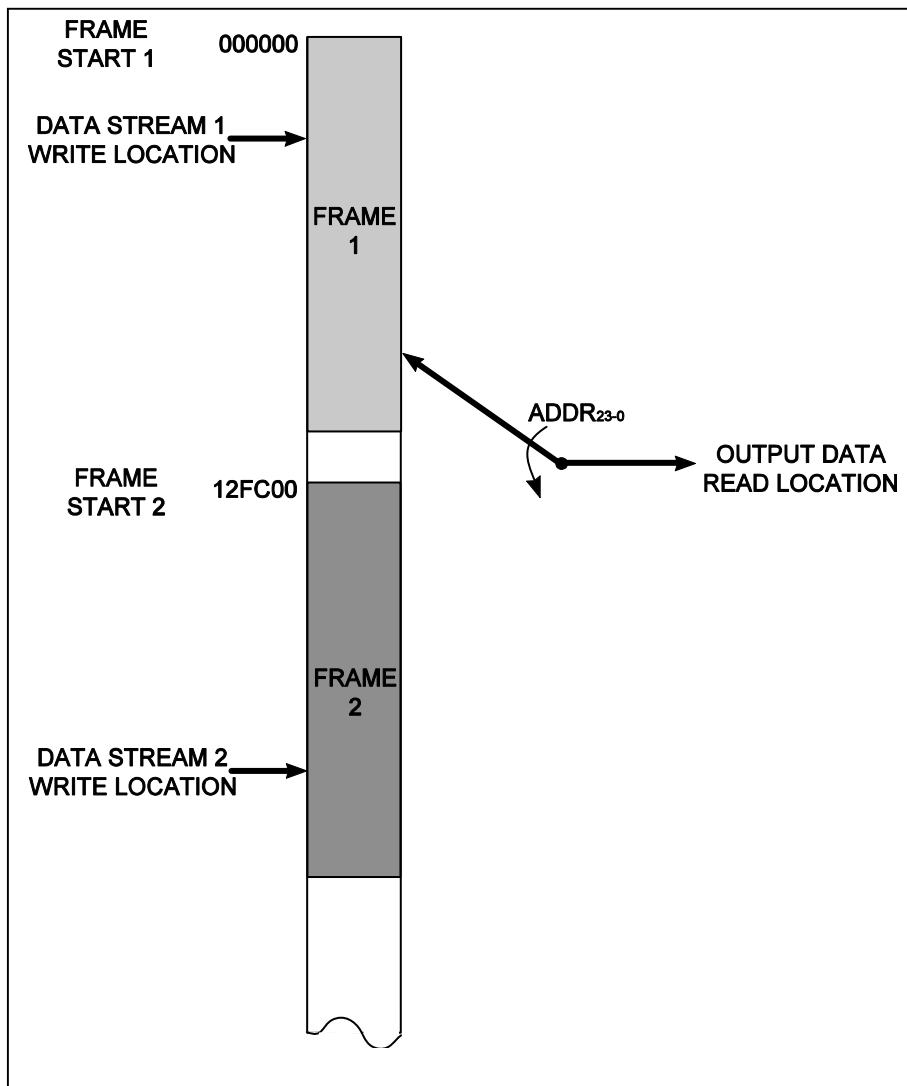


## OVERVIEW

Multiple independent data/video streams can be written into a shared linear address space using multiple LF3312s. Picture in Picture applications can be implemented where multiple video feeds are buffered simultaneously yet the data can be view/read as if it was stored in one single memory with a single shared address space. A PIP solution using LF3312s can buffer and synchronize up to 16 independent video/data streams.

This is made possible by placing N LF3312s in a 'semi-cascade' mode, where all inputs and outputs are tied together - except for the 12bit AIN input ports and ASET write pointer control pins, which remain independent. In this manner, each device is responsible for 1/N of the shared memory address space. The single read address can be manipulated full-time (in a random access manner) using the 24bit BOUT/BIN address port – having access to the total address space.

In order to reference the start of a frame of video with a specific address within the shared space, each external video stream's Frame Sync must be tied to its respective device's ASET (write pointer SET control). This will jump the write pointer back to the appropriate 'frame start' address at the beginning of every subsequent frame boundary – and then continue incrementing sequentially.



The figure to the left shows the address space of 2 devices cascaded in 10bit mode (a single LF3312 has 1,244,160 or 12FC00hex locations in 10bit mode).

Since their input data ports and write-addresses are independent, we show two unique write pointers 1 & 2 – and a single read pointer that has access to the total address space. Note that each input stream of data can be totally asynchronous to each other.

When cascading LF3312 devices, each individual device in the cascade writes/reads based on what the current write/read pointer is and where that device fits within the cascade (Chip 1 of 4, Chip 2 of 4, etc...). Configuration Register C[3:0] (BASE\_ADDR) is used to define each device's place in the cascade and Configuration Register C[7:4] (CASCADE) is used to define the number of devices in cascade.

For example, in 10bit mode, each LF3312 has 1,244,160 address locations (0 to 12FBFF). When the cascade's common write pointer is between address 0 and 12FBFF, the device with BASE\_ADDR=0 actively writes into its memory. When the common write pointer either advances, or is SET to an address in the 12FC00 to 25F7FF region, the device with BASE\_ADDR=1 actively writes into its memory. Reading from memory works in the same fashion.

When cascading LF3312s, only single-channel modes are supported (OPMODES 0 to 3). The write enables AWEN/BWEN and AIEN/BIEN must be tied together for each device. All read enables AREN/BREN for the entire cascade must be tied together (see the device connection diagram on the next page).

For multi-source cascading, the configuration registers of each device must be programmed identically, depending on mode/function, except for Register 2, 3, 4, and C. Registers 2, 3, and 4 define ALATENCY, which in this application defines the 'Frame Start' address. Register C defines which region of the 24bit address space the particular device is responsible for. Within Register C, there is a 4bit BASE\_ADDR and 4bit CASCADE word. BASE\_ADDR determines the region of address space each device controls, and CASCADE defines how many devices are in cascade.

Example) 3 devices cascaded. Each device's Register C programmed as the following:

#### CHIP 0

Configuration Register Address	Data[7:0]	Description
C	02	Chip 0 out of 3 devices in cascade

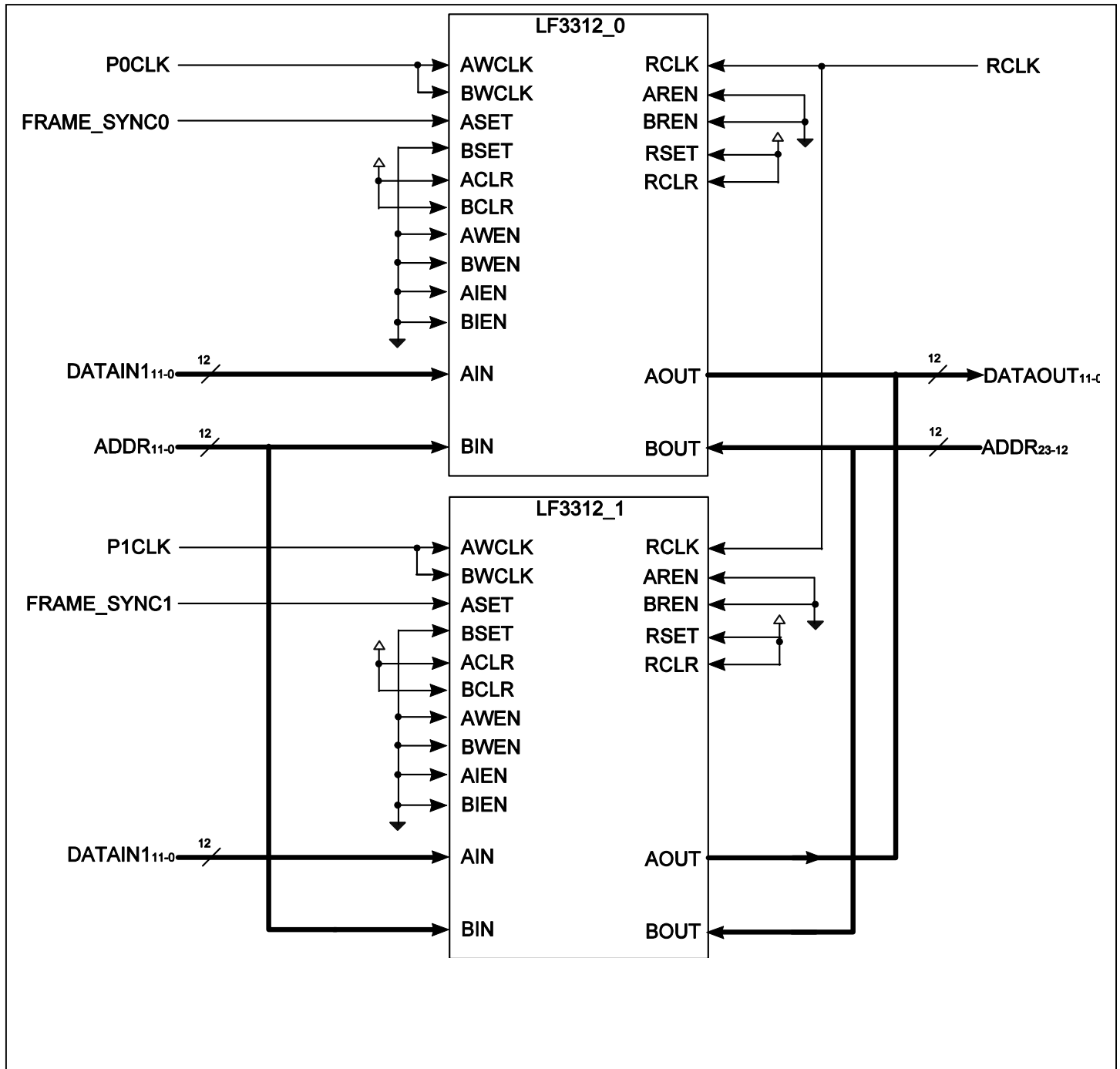
#### CHIP 1

Configuration Register Address	Data[7:0]	Description
C	12	Chip 1 out of 3 devices in cascade

#### CHIP 2

Configuration Register Address	Data[7:0]	Description
C	22	Chip 2 out of 3 devices in cascade

Application: Two Cascaded LF3312s – 2-frame PIP or Multi-source Buffering Connection



In the above application diagram, 2 sources of 12bit video DATAIN0 and DATAIN1 are written to memory, using their respective frame syncs (FRAME\_SYNC0 and FRAME\_SYNC1) as timing signals. The 24bit address port accesses the entire memory space and is used for determining which pixels to read out. BSET and BCLR pins select the source of an address jump. The write pointer jumps to the address located in ALATENCY after ASET is asserted, and the read pointer jumps to the address specified by the 24bit ADDR port when RSET is asserted.

The following table of pin-tie-offs is true for Chip n of N.

PIN	TIE-OFF	DESCRIPTION
AWCLK	----	Connect to external video source clock n
BWCLK	Tie to AWCLK	Tied to AWCLK
RCLK	----	Connect all RCLKs to master video clock
AIN	----	Connect to external video data source n
BIN	----	ADDR[11:0] of common 24bit read address port
CHIP_ADDR	Tie all bits LOW	Serial interface ID bits not used
SCL	Tie HIGH	Not using serial interface
PADDR	----	Used for parallel interface
PDATA	----	Used for parallel interface
SDA	Tie HIGH	Not using serial interface
BOUT	UNCONNECTED	Not Used
ACLR	Tie HIGH	Not used in this example
BCLR	Tie HIGH	Read address uses BIN/BOUT
ASET	----	Connect to video source n frame sync
BSET	Tie LOW	Write address uses ALATENCY
AMARK	Tie HIGH	Not used in this example
BMARK	Tie HIGH	Not used in this example
RSET	Tie LOW	Forces read address to always be controlled by 24bit BIN/BOUT
RCLR	Tie HIGH	Not used in this example
AWEN	Tie LOW	This example expects continuous input data stream
BWEN	Tie to AWEN	In single channel mode, always tie to AWEN
AIEN	Tie LOW	Always writing to memory
BIEN	Tie LOW	Always writing to memory
AREN	Tie LOW	This example expects continuous output data stream
BREN	Tie to AREN	In single channel mode, always tie to AREN
PROGRAM	Tie HIGH	This example uses parallel interface
LOAD	----	LOW at start of operation, bring HIGH after configuration
RESET	----	LOW for $\geq 1$ cycles prior to configuration (while LOAD is LOW)
AOE	Tie LOW	This example never disables AOUT
BOE	Tie HIGH	BOUT is an input
CSB	----	Used for parallel interface
WEB	----	Used for parallel interface
REB	----	Used for parallel interface

The table outlines the configuration data/addresses for Chip 0 of 2 (LF3312\_0)

Configuration Register Address	Data[7:0]	Description
2	00	FRAME_START_ADDRESS[23:16]
3	00	FRAME_START_ADDRESS[15:8]
4	00	FRAME_START_ADDRESS[7:0]
8	C1	Random Access mode, 12bit data word
9	08	Enable read pointer to be forced to a specific address
C	01	Chip 0 of 2 cascaded devices

The table outlines the configuration data/addresses for Chip 1 of 2 (LF3312\_1)

Configuration Register Address	Data[7:0]	Description
2	12	FRAME_START_ADDRESS[23:16]
3	FC	FRAME_START_ADDRESS[15:8]
4	00	FRAME_START_ADDRESS[7:0]
8	C1	Random Access mode, 12bit data word
9	08	Enable read pointer to be forced to a specific address
C	11	Chip 1 of 2 cascaded devices