

OVERVIEW

The LF3312 has been designed to support flexible manipulation of the Write and Read pointers. Each write and read pointer, whether in single or dual memory channel mode, can be set/jumped to a specified address anywhere within the address space of the memory. Jumping these pointers to any arbitrary address location is also supported in cascade mode – where a seamless address space is maintained regardless of the number of LF3312 cascaded devices. There are dynamic control pins such as ACLR, BCLR, RLCR, ASET, BSET, and RSET that can be used to ‘jump’ the W/R pointers to specific addresses. Due to the sheer number of possibilities of manipulating the Write and Read pointers with the LF3312, this application brief should be a helpful appendix to the datasheet.

This document breaks ‘Pointer Manipulation’ into 3 sections; simple pointer clearing, random access using the external address port, and pointer jumping using internal configuration registers.

It should be first pointed out that in all modes, the W/R pointers in the LF3312 are inherently based on the FIFO-style of being sequentially incremented. The LF3312, however, enables the user to dynamically adjust his/her addressing methods from the fully random-access cycle-by-cycle addressing to jumping the pointers to a specified address and letting the pointers resume a sequential address path.

Also, it is important to note that the LF3312 memory should be viewed as a linear address, yet it can be allocated into variable length Rows, Lines, or Queues when in single-channel modes. That is, it can be addressed as a Cartesian coordinate address space with a Row/Column address (or Y/X address). The LF3312’s 24bit address space, when allocated in a Cartesian coordinate system consists of 12MSBs as the Y address and the 12LSBs as the X address.

$$24\text{bit Linear Address} = (Y \times \text{ROWLENGTH}) + X$$

As a side note, when ROWLENGTH is zero, the Y address is effectively multiplied by 4096, resulting in a full 24bit linear address space. For example, in 10bit mode the memory contains 1,244,160 words that can be allocated as a linear address space from 0 to 1244159 (ROWLENGTH Register set to 0 – which is its default setting). This same memory space can store a frame of video having 1280 pixels/line and storing up to 970 lines (ROWLENGTH Register set to 500hex). When cascading multiple LF3312s, this seamless Cartesian coordinate address space is maintained, only more Rows (or lines of video) can be stored and accessed.

NOTE: If pointer jumping or clearing is desired using the LF3312 as a single memory channel, it is recommended that the device be placed in a specific random-access operational mode (OPMODE[2:0]=010). Other single channel modes may inadvertently disable the read pointer based on perceived distances between W/R pointers.

NOTE: In single-channel modes, AWEN and BWEN must be tied together, as must AREN/BREN, AIEN/BIEN, and AWCLK/BWCLK. In dual-channel modes, Channel A and Channel B Write and Read enables and clocks are all independent.

NOTE: the methods of jumping and clearing of the pointers described below are supported in all operational modes (OPMODE Register 8[2:0]).

CLEARING THE WRITE/READ POINTERS

The simplest jumping of pointers is in clearing the write and read pointers to address 0. Predefined pins ACLR, BCLR, and RCLR exist to perform this task.

In single channel mode or when cascading multiple devices, ACLR alone resets the Write pointer. AWENB and BWENB must be active (LOW) for 2 cycles before ACLR is asserted. ACLR can be programmed to be falling edge or level sensitive (Register A).

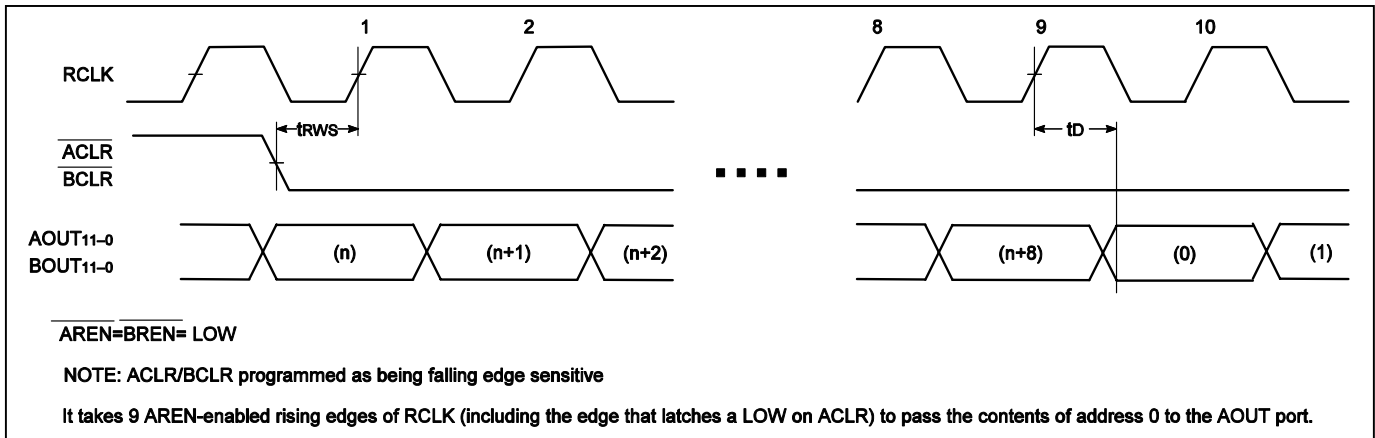
In dual channel mode, ACLR resets the Write pointer of Channel A and BCLR resets the Write pointer of Channel B. AWEN and BWEN must be active (LOW) for 2 cycles before asserting ACLR and BCLR respectively. Both ACLR and BCLR can be programmed to be falling edge or level sensitive (Register A).

NOTE: any ACLR or BCLR assertion has priority over a simultaneous RSET event.

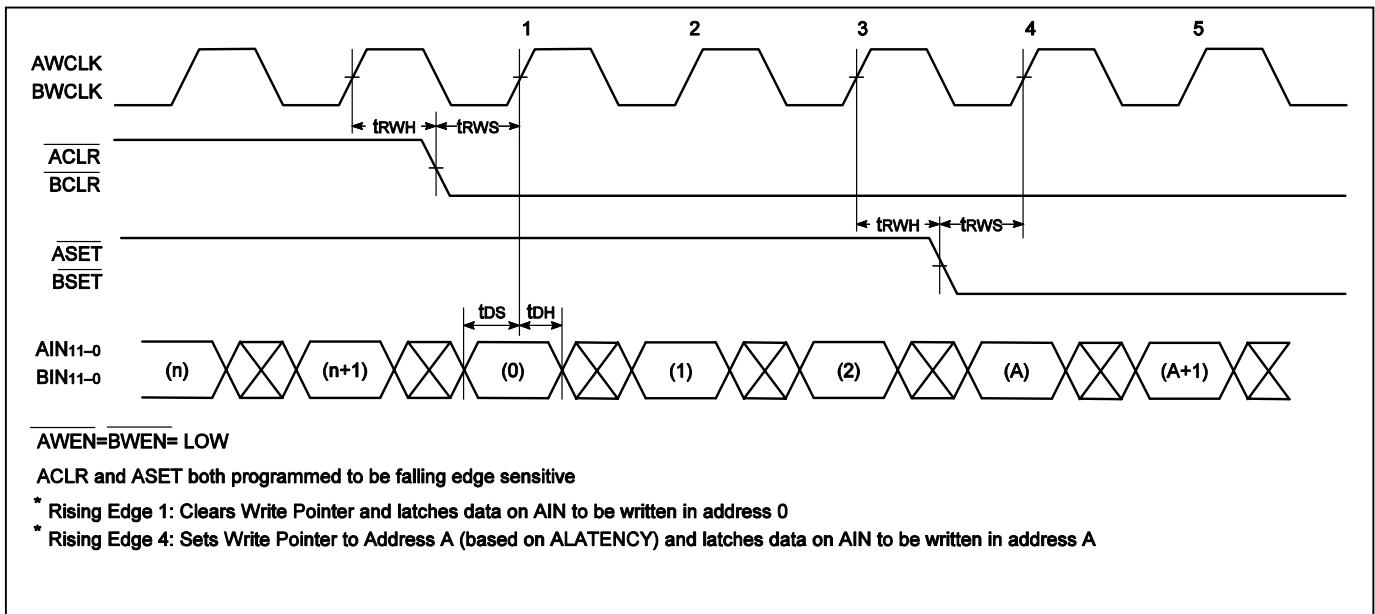
In either single or dual channel mode or when cascading multiple devices, RCLR resets the Read pointer. In single-channel mode, RCLR requires both AREN and BREN to be active (LOW) for 1 cycle before being asserted – clearing the read pointer to zero. In dual-channel mode, AREN controls the effectiveness of RCLR on resetting Channel A's read pointer and BREN controls the effectiveness of RCLR on resetting Channel B's read pointer. Again, AREN and BREN must be active (LOW) for 1 cycle before bringing RCLR LOW. RCLR can be programmed to be falling edge or level sensitive (Register A).

Upon bringing RCLR LOW, the Read pointer is immediately set to zero. It takes 9 AREN-enabled rising edges of RCLK for the contents of address 0 to arrive on AOUT after bringing RCLR LOW. Similarly, it takes 9 BREN-enabled rising edges of RCLK for the contents of Channel B's address 0 to arrive on BOUT after bringing RCLR LOW, when in dual-channel mode.

Read Pointer Clear



Write Pointer Clear



RANDOM ACCESS - W/R POINTER CONTROL BASED ON EXTERNAL ADDRESS

In addition to jumping the W/R pointers based on a static address contained in a configuration register, the LF3312 allows the user to dynamically force the write pointer to an address based on an external 24bit address port on a cycle-by-cycle basis. This feature allows true random access writing or reading to occur.

The 24bit address port uses the two 12bit BIN/BOUT ports, and **therefore can only be used in single-channel mode**. Since only one 24bit address bus is supplied, full time random access can be performed on a full-time basis for either the Write or Read pointer. However, this address port can serve both read and write pointers at different times. In addition to forcing the pointers to the 24bit external address on a full-time basis, the LF3312 can use this address as a 'jump' address whereby the write or read pointer can be jumped to it, and then released to continue its natural sequential addressing. This can be useful if the W/R pointers need to jump throughout a large number of 'virtual regions' in the memory space, or if one needs to jump the pointers across these regions dynamically on a cycle-by-cycle basis.

NOTE: In single channel modes, BCLR and BSET control the source of the Write and Read 'jump address' triggered by the ASET and RSET write and read address jump controls. In these modes, BCLR is registered with RCLK and enabled by AREN. BSET is registered with AWCLK and AWEN. When switching BSET and/or BCLR to change the source of the 'jump' address, one must make sure that a rising edge of AWCLK (enabled by AWEN) and/or a rising edge of RCLK (enabled by AREN) latches the change in the source-selector. If not, the internal 'address source-selector' will not have been updated. AWEN must be LOW 2 rising edges before latching the BSET transition. AREN must be LOW 1 rising edge before latching the BCLR transition.

NOTE: When using the BIN and BOUT ports as an address port, be sure to bring BOE HIGH, tri-stating the BOUT port and allowing it to become an input.

Controlling the Write Pointer with the 24bit BIN/BOUT Address

BSET must be brought HIGH in order for the BIN/BOUT port to be selected as the 24bit write address source. Once BSET is HIGH, bringing the ASET pin LOW forces the Write pointer to the 24bit address defined by BIN/BOUT upon a rising edge of AWCLK/BWCLK. The BIN/BOUT address must be valid only as long as ASET remains LOW. The BIN/BOUT address is latched on the rising edge of AWCLK/BWCLK and enabled by AWEN/BWEN in this mode (single channel mode with BSET=1). AWEN/BWEN must be brought LOW 2 cycles before the valid 24bit address, sitting on BIN/BOUT, is triggered by bringing ASET LOW. AWEN/BWEN enables both the BIN/BOUT address and ASET event. The BIN/BOUT address must be valid only as long as ASET remains LOW.

Bringing ASET LOW for only one cycle (ASET programmed to be level sensitive) effectively jumps the Write pointer to the address described by BIN/BOUT and sequentially increments from that point forward (until ASET is brought LOW again). In the case that ASET is falling edge sensitive, simply bringing ASET LOW results in the same pointer behaviour as above without requiring it to be LOW for exactly one cycle.

Leaving ASET LOW for multiple cycles (ASET programmed to be level sensitive) allows full-time Random Access control of the Write pointer. Through this sort of addressing, the 24bit address described by BIN/BOUT can be changed every cycle if desired.

ASET can be programmed to be falling edge or level sensitive (Register A).

NOTE: For the first address jump using the BIN/BOUT method, the 7-cycle pipeline of Address/Data must be filled. Without filling this pipeline, the first jump will not occur. AWEN and BWEN must be brought LOW at least 7 rising edges of AWCLK prior to rising edge of AWCLK that latches in the first valid data word and BIN/BOUT address.

Controlling the Read Pointer with the 24bit BIN/BOUT Address

BSET must be brought LOW and BCLR must be brought HIGH in order for the BIN/BOUT ports to be selected as 24bit read address source. Once BSET=0 and BCLR=1, bringing the RSET pin LOW forces the Read pointer to the 24bit address defined by BIN/BOUT upon a rising edge of RCLK. The BIN/BOUT address is latched on the rising edge of RCLK and enabled by AREN/BREN in this mode (single channel mode with BSET=0 and BCLR=1). AREN/BREN and must be LOW 1 cycle before the valid 24bit address, sitting on BIN/BOUT, is triggered. The BIN/BOUT address must be valid only as long as RSET remains LOW.

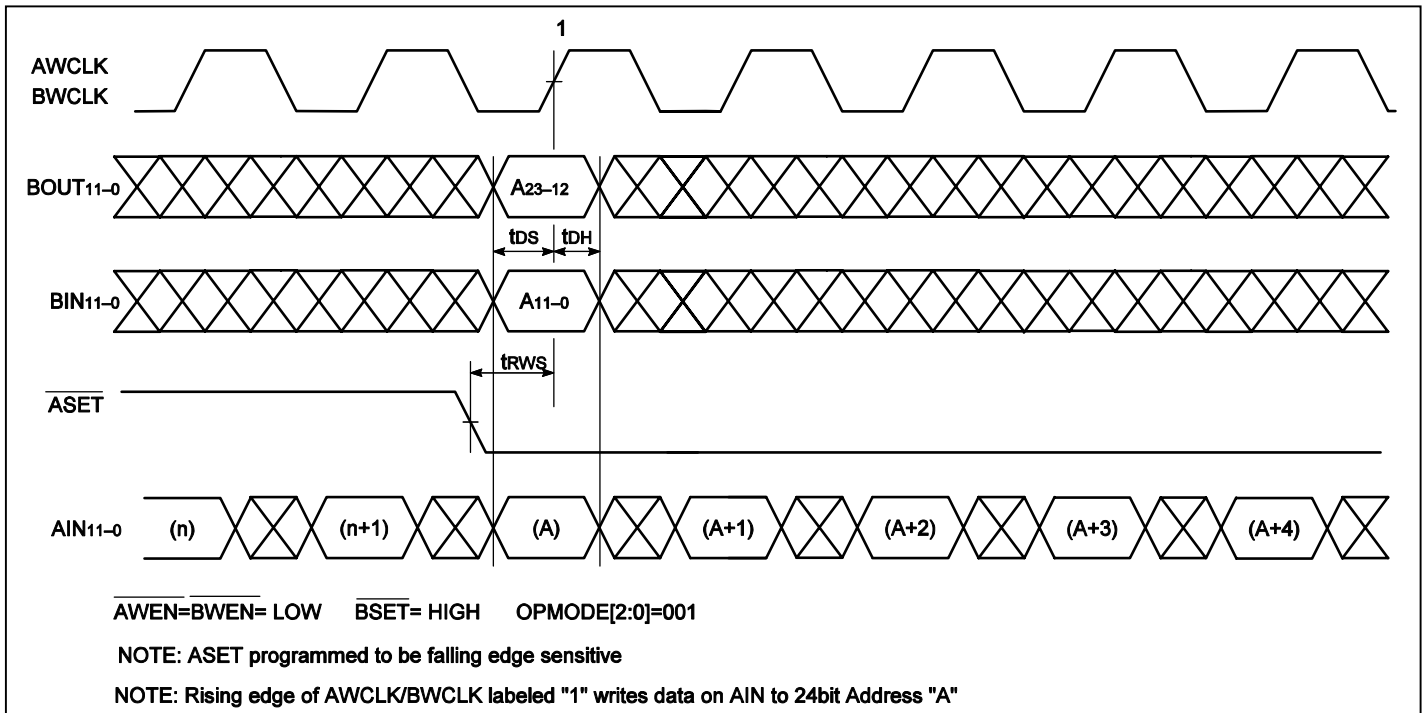
Bringing RSET LOW for only one cycle (RSET programmed to be level sensitive) effectively jumps the Read pointer to the address described by BIN/BOUT and sequentially increments from that point forward (until RSET is brought LOW again). In the case that RSET is falling edge sensitive, simply bringing RSET LOW results in the same pointer behaviour as above without requiring it to be LOW for exactly one cycle.

Leaving RSET LOW for multiple cycles (RSET programmed to be level sensitive) allows full-time Random Access control of the Read pointer. Through this sort of addressing, the 24bit address described by BIN/BOUT can be changed every cycle if desired.

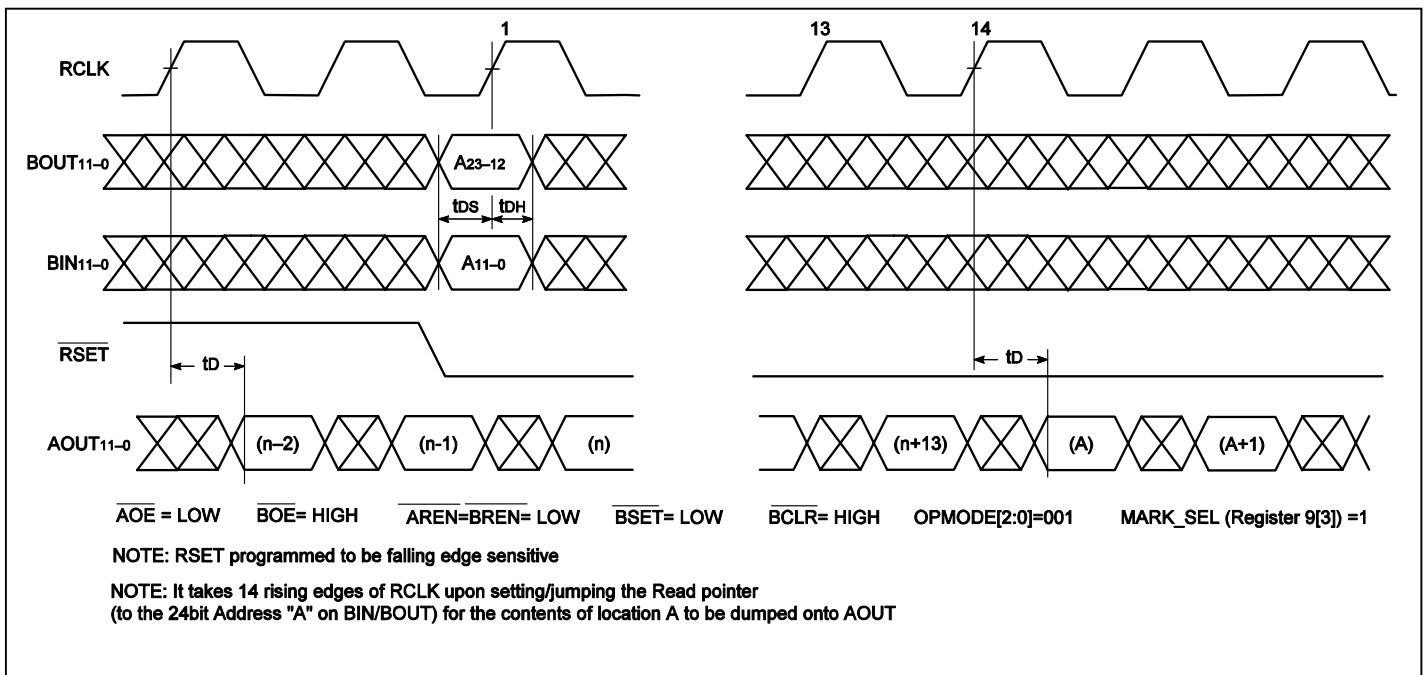
RSET can be programmed to be falling edge or level sensitive (Register A).

NOTE: For the first address jump using the BIN/BOUT method, the 7-cycle pipeline of Address/Data must be filled. Without filling this pipeline, the first jump will not occur. AWEN and BWEN must be brought LOW at least 7 rising edges of AWCLK prior to rising edge of AWCLK that latches in the first valid data word and BIN/BOUT address.

Write Pointer Jumping using BIN/BOUT



Read Pointer Jumping using BIN/BOUT



JUMPING W/R POINTERS TO ADDRESSES PRE-LOADED IN CONFIG. REGISTERS

The LF3312 allows the user to jump the write pointer to a specific address and then release pointer to resume its sequential increment. Jumping the Write or Read pointer to an address contained in a Configuration register can be useful if a limited number of 'virtual regions' in the memory space have been allocated, if one does not need to switch between these regions dynamically on a cycle-by-cycle basis, or if board signal traces must be minimized.

Since there is a limited number of registers available for storing pre-defined 'region addresses', nearly every application will require the register to be preloaded, using either of the two interfaces, with the appropriate address prior to each W/R pointer jump.

Just after updating the register, an internal process must be triggered to remap the 24bit register address into an internal memory 'jump' address. It is described below.

Jumping the Write and/or Read Pointer to a Pre-defined Address

In single-channel mode the pin that controls the source of the 'write pointer jump' address is BSET. When BSET is LOW, the ALATENCY 24bit register is used as the 24bit linear write-jump address. For every different address that the Write pointer is to be jumped to, this ALATENCY register must be preloaded and updated. Bringing ASET LOW forces the write pointer to the preloaded address and writes the data sitting on AIN to the specified address. Assuming the write address is released, the write pointer continues with address+1, etc. ASET can be programmed to be falling edge or level sensitive (Register A).

In single-channel mode the pin that controls the source of the 'read pointer jump' address is BCLR. When BCLR is LOW, the BLATENCY 24bit register is used as the 24bit linear read-jump address. For every different address that the Read pointer is to be jumped to, this BLATENCY register must be updated prior to the jump/set. Bringing RSET LOW forces the read pointer to the preloaded address. Assuming the read address is released, the read pointer continues with address+1, etc. RSET can be programmed to be falling edge or level sensitive (Register A).

Remapping of the 24bit linear ALATENCY or BLATENCY address, loaded into configuration register(s), must be triggered before they are used. The following 'remap trigger' sequence involving LOAD and AWEN/BWEN must be observed, since a LOAD transition triggers while AWEN enables this sequence. There are two methods for handling LOAD when updating either of the ALATENCY/BLATENCY register addresses.

CASE1 – keeping LOAD LOW the duration of loading the registers through the interface and bringing it back HIGH when finished.

CASE 2 – using the double-buffered configuration registers; loading the registers transparently to the device while LOAD is HIGH, and pulsing LOAD LOW to update the working registers.

Upon completion of loading either register, LOAD must be brought HIGH (CASE 1) or LOAD must be brought LOW (CASE 2). The transition on LOAD triggers the remapping. Since AWEN enables the remapping it must be brought LOW prior to the LOAD transition and be kept LOW for a number of

cycles afterwards. In either CASE, AWEN must be LOW for a minimum of 3 cycles prior and 5 cycles after the LOAD transition.

A few cycles after the LOAD transition, the read/write pointer can be jumped/set after waiting a minimum number of cycles for the remap process to finish.

- ASET can jump the write pointer to ALATENCY (BSET=0) a minimum of 2 rising edges of AWCLK after LOAD transition (single channel modes)
- RSET can jump the read pointer to BLATENCY (BCLR=0) a minimum of 6 rising edges of RCLK after LOAD transition (single-channel modes)
- BSET can jump the Ch. B write pointer to BLATENCY a minimum of 6 rising edges of BWCLK after LOAD transition (dual channel modes),
- RSET can jump the read pointer to BLATENCY a minimum of 6 rising edges of RCLK after LOAD transition (dual-channel modes),

It should be noted that the above cycles are a minimum. The ALATENCY/BLATENCY registers can be loaded far in advance of being used.

Single Channel Modes:

The control pin that sets the write pointer to the predefined address is ASET. AWEN must be active (LOW) for 2 cycles before ASET can be asserted. ASET can be programmed to be falling edge or level sensitive (Register A).

The control pin that sets the read pointer to the predefined address is RSET. AREN must be active (LOW) for 1 cycle before RSET can be asserted. RSET can be programmed to be falling edge or level sensitive (Register A).

From an assertion of RSET, it takes 14 read-enabled (AREN/BREN) rising edges of RCLK (including the edge that latches a LOW on RSET) to produce valid data on AOUT from the contents of the predefined address.

Dual Channel Modes:

The control pin that sets the Channel A write pointer to the predefined address is ASET. AWENB must be active (LOW) for 2 cycles before ASET can be asserted. ASET can be programmed to be falling edge or level sensitive (Register A).

The control pin that sets the Channel B write pointer to the predefined address is BSET. BWENB must be active (LOW) for 2 cycles before BSET can be asserted. BSET can be programmed to be falling edge or level sensitive (Register A).

The control pin that sets the Channel A read pointer to the predefined address is RSET. AREN must be active (LOW) for 1 cycle before RSET can be asserted. RSET can be programmed to be falling edge or level sensitive (Register A).

The control pin that sets the Channel B read pointer to the predefined address is also RSET. BREN must be active (LOW) for 1 cycle before RSET can be asserted. RSET can be programmed to be falling edge or level sensitive (Register A).

From an assertion of RSET, it takes 14 AREN-enabled rising edges of RCLK (including the edge that latches a LOW on RSET) to produce valid data on AOUT from the contents of the predefined address on Channel A.

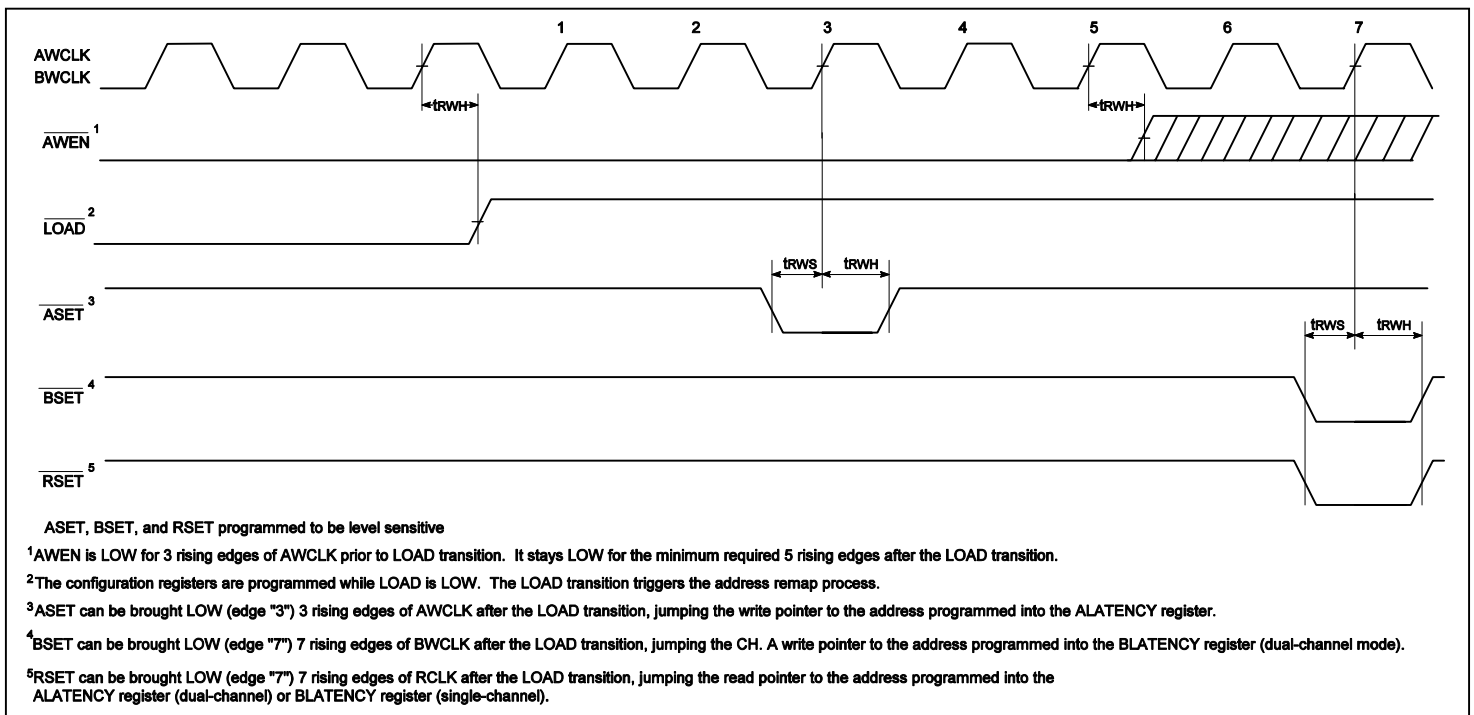
From an assertion of RSET, it takes 14 BREN-enabled rising edges of RCLK (including the edge that latches a LOW on RSET) to produce valid data on BOUT from the contents of the predefined address on Channel B.

NOTE: When using the RSET to jump the Read pointer to a location there is no limit on a minimum number of samples to read sequentially before jumping to a new location – however it does take 6 cycles for the BLATENCY configuration register address to be remapped to a valid internal memory address, which effectively sets a minimum number of samples to 6+(number of RCLK cycles it takes to program the BLATENCY register with the MCU interface).

NOTE: When reading amongst multiple regions of memory, seamless region-switching is done by preloading the desired BLATENCY address, and asserting RSET 14 RCLK cycles before the first sample of the new region is expected. That is, data remains valid on the AOUT regardless of the read pointer being jumped from one region to another.

NOTE: during an assertion of RSET, the determination of which channel's pointer is to be jumped is dependent on which channel's read enable (AREN or BREN) is active. For example, if ONLY channel A's read pointer is to be jumped, channel B's BREN must be disabled.

Jumping Pointers using Config. Register Address after Remapping Process



SINGLE-CHANNEL POINTER JUMP CONTROLS (OPMODES 0-3)

WRITE POINTER 'JUMP ADDRESS' SOURCE

BSET	Triggered by bringing ASET LOW (AWEN must be LOW)
0	ALATENCY – 24bit predefined configuration register
1	BIN/BOUT – 24bit external address port

READ POINTER 'JUMP ADDRESS' SOURCE

MARKSEL	BSET	BCLR	Triggered by bringing RSET LOW (AREN must be LOW)
1	0	0	BLATENCY – 24bit predefined configuration register
1	0	1	BIN/BOUT – 24bit external address port
1	1	0	BLATENCY – 24bit predefined configuration register
1	1	1	INVALID
0	X	X	MARKED Address (write address marked by AMARK)

WRITE POINTER RESET / CLEAR

CONTROL	Write Pointer Clear Location
Triggered by Bringing ACLR LOW (AWEN is LOW)	00000 (zero)

READ POINTER RESET / CLEAR

CONTROL	Read Pointer Clear Location
Triggered by Bringing RCLR LOW (AREN is LOW)	00000 (zero)

DUAL-CHANNEL POINTER JUMP CONTROLS (OPMODES 4-7)

Ch. A WRITE POINTER JUMPS

CONTROL	Write Pointer Jump Location
Triggered by Bringing ASET LOW (AWEN is LOW)	ALATENCY (predefined)

Ch. B WRITE POINTER JUMPS

CONTROL	Write Pointer Jump Location
Triggered by Bringing BSET LOW (BWEN is LOW)	BLATENCY (predefined)

Ch. A WRITE POINTER CLEARS

CONTROL	Write Pointer Jump Location
Triggered by Bringing ACL LOW (AWEN is LOW)	00000 (zero)

Ch. B WRITE POINTER CLEARS

CONTROL	Write Pointer Jump Location
Triggered by Bringing BCL LOW (WWEN is LOW)	00000 (zero)

Ch. A READ POINTER JUMPS

CONTROL	Read Pointer Jump Location
MARKSEL	Triggered by RSET = LOW (BREN is LOW)
0	AMARKED Addr.
1	ALATENCY

Ch. B READ POINTER JUMPS

CONTROL	Read Pointer Jump Location
MARKSEL	Triggered by RSET = LOW (BREN is LOW)
0	BMARKED Addr.
1	BLATENCY

Ch. A READ POINTER CLEARS

CONTROL	Read Pointer Jump Location
Triggered by Bringing RCL LOW (AREN is LOW)	00000 (zero)

Ch. B READ POINTER CLEARS

CONTROL	Read Pointer Jump Location
Triggered by Bringing RCL LOW (BREN is LOW)	00000 (zero)

LATENCIES

SIGNAL	LATENCY	DESCRIPTION
AWEN	2	Bring LOW # rising xWCLK edges prior to valid input data (AIN)
BWEN	2	Bring LOW # rising xWCLK edges prior to valid input data (AIN / BIN)
AIEN	2	Bring LOW # rising xWCLK edges prior to valid input data (AIN)
BIEN	2	Bring LOW # rising xWCLK edges prior to valid input data (AIN / BIN)
AREN	1	Bring LOW # rising xRCLK edges prior to expecting new valid output data
BREN	1	Bring LOW # rising xRCLK edges prior to expecting new valid output data

SIGNAL	LATENCY	DESCRIPTION (NOTE: 24bit Address N=BIN/BOU or N=ALATENCY or N=BLATENCY)
ASET	1	Rising edge of WCLK that latches LOW on ASET also points current AIN sample to Address N
ACLR	1	Rising edge of WCLK that latches LOW on ACLR also points current AIN sample to Address 0
RCLR	9	Rising edges of RCLK (including edge that latches LOW on RCLR) to Address 0 on AOUT
RSET	14	Rising edges of RCLK (including edge that latches LOW on RSET) to Address N on AOUT