

OVERVIEW

The RESET pin can both reset the contents of the Configuration Registers back to their default states (see datasheet) and act as a 'global W/R pointer reset'.

There are two types of resets that can be accomplished using the RESET pin: Hard and Soft resets.

The Hard reset affects both the configuration registers and the W/R pointers, whereas the Soft reset only affects the W/R pointers.

Reset	DESCRIPTION	Bring RESET LOW
HARD	<ul style="list-style-type: none"> ▪ All configuration registers are reset to their default states 	While LOAD is LOW
	<ul style="list-style-type: none"> ▪ All W/R pointers are reset to zero 	
SOFT	<ul style="list-style-type: none"> ▪ Configuration registers remain unchanged 	While LOAD is HIGH
	<ul style="list-style-type: none"> ▪ All W/R pointers are reset to zero 	

In order to issue a HARD Reset, bring RESET LOW while LOAD is LOW.

In order to issue a SOFT Reset, bring RESET LOW while LOAD is HIGH.

Both reset events are synchronous, however AWCLK, BWCLK and RCLK all latch the single RESET and provide resets for their respective pointers/registers. That is, although the RESET pin is brought LOW, a rising edge of clock is still necessary for the reset to be issued.

While issuing a HARD reset in single-channel mode, a rising edge of AWCLK resets the Write pointer and a rising edge of RCLK resets the Read pointer.

While issuing a HARD reset in dual-channel mode, a rising edge of AWCLK resets the Channel A Write pointer, a rising edge of BWCLK resets the Channel B Write pointer, and a rising edge of RCLK resets both channel's Read pointers.

NOTE: A global reset of the Write and Read pointers is independent of operational mode.