LOGIC DEVICES INCORPORATED

Frame Delay of Digital Component Video
LF3312 - Application Note

OVERVIEW

It is sometimes necessary to buffer fields or frames in a completely synchronous, delay-line fashion. This is often the case when comparing the current frame (f) with previous frames (f-1), (f-2), and so on. The LF3312's Synchronous Shift Register Mode automatically sets a user-defined distance between the Write and Read pointers, setting the latency between AIN and AOUT. In dual-channel shift register mode, 2 independent shift-registers in a single device, with Channel A I/O ports supported by AIN and AOUT and Channel B I/O ports supported by BIN and BOUT.

After the device is programmed and triggered to begin operation, the write pointer advances until a counter (set to the user-defined latency) reaches the desired count, at which point the read pointer begins to advance.

THE DETAILS

Since both writing and reading must be done synchronously, and since the LF3312 has a single Read-clock, all W/R clocks must be tied together. AWCLK, BWCLK, and RCLK must be tied together regardless of the number of desired channels to be buffered within the device (single or dual channels).

In single-channel shift register mode, the write enables AWEN/BWEN must be tied together. Similarly, the read enables must be tied together.

The write and read enables, AWEN/BWEN and AREN/BREN, can be hardwired LOW the entire operation of the shift register if neither the write or read pointers will be required to stop or halt at any point. The write and read pointers can also be brought LOW when valid data is finally sitting on the AIN port.

The 24bit ALATENCY register should be programmed to the desired total latency between AIN and AOUT. In dual-channel mode, the latency between BIN and BOUT is determined by the 24bit BLATENCY register.

The table below outlines the total latency that the LF3312 exhibits under different handling of the AWEN/BWEN/AREN/BREN write/read enables.

Just prior to programming the configuration registers, LOAD should be brought LOW. RESET should be toggled LOW to trigger a global reset (which resets the pointers and sets the configuration registers to their default states). RESET is then brought HIGH the registers programmed, in this case using the parallel interface. Upon completion of programming, LOAD must be brought HIGH – which triggers the user-defined latency 'counter' if/when AWEN/BWEN are brought LOW.

SHIFT REGISTER LATENCY SETTINGS		
Channel	**W/R Enable Initialization**	**Total IN-OUT Latency**
A	Ch. A Write and Read enables tied LOW	32+ALATENCY
A	Ch. A Write and Read enables HIGH then brought LOW for data	30+ALATENCY
B	Ch. B Write and Read enables tied LOW	32+BLATENCY
B	Ch. B Write and Read enables HIGH then brought LOW for data	30+BLATENCY

APPLICATION: FRAME DELAY OF DIGITAL COMPONENT VIDEO

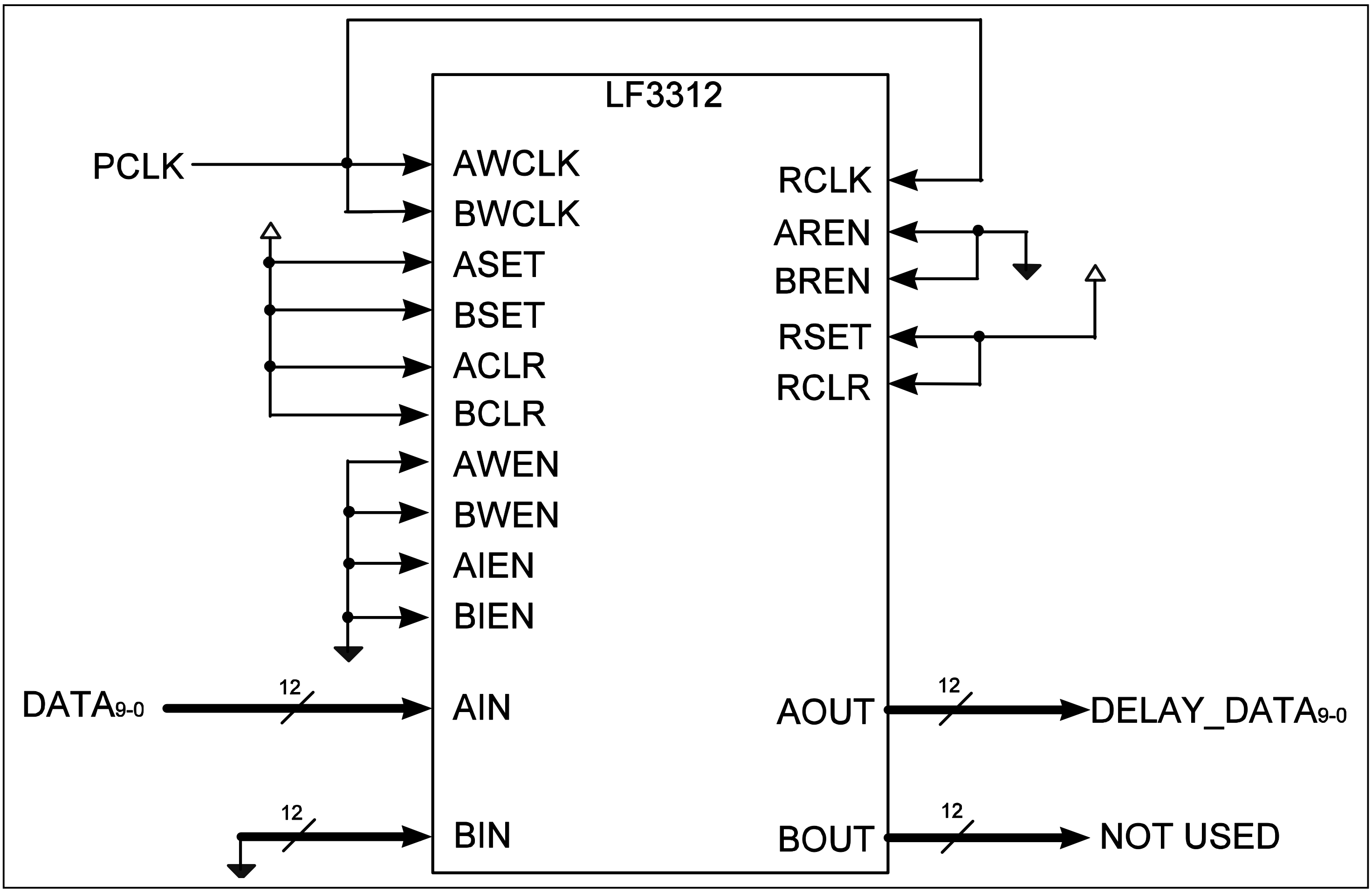
In the following application, we will provide a full frame synchronous delay line for an ITU-R BT.601 525/60 video system in 10bits. The full frame consists of 1716 total samples x 525 lines = 900,900 samples of delay. We place the LF3312 in single-channel shift register mode (OPMODE=000) with 10bit data (WIDTH=10). The AWCLK/BWCLK/RCLK are tied to the 27MHZ video clock.

Since this example has assumed that writes and reads happen continuously, we tie AWEN/BWEN/AREN/BREN all LOW. The desired latency is 900,900 samples, and therefore we load ALATENCY as "desired_latency – 32" which is 900,868 or DBF04 hex.

Just prior to programming the configuration registers, LOAD will be brought LOW. RESET will be toggled LOW for a cycle or more to trigger a global reset (which resets the pointers and sets the configuration registers to their default states). We then bring RESET HIGH and program the registers, in this case using the parallel interface. Upon completion of programming, LOAD is brought HIGH – which triggers the user-defined latency 'counter', since AWEN/BWEN are to be LOW the entire operation of the device.

The data path will exhibit a "ALATENCY-32" delay, after the internal counter counts "ALATENCY-32" cycles – triggering the read pointer to begin following the write pointer.

The tables on the next page outline the pin and configuration settings suggested for this application.



PIN	INITIALIZE	DESCRIPTION
AWCLK	----	Connect to external video source clock
BWCLK	Tie to AWCLK	In single channel modes, always tie to AWCLK
RCLK	Tie to AWCLK	All clocks are tied together
AIN	----	Connect to external video data source
BIN	Tie HIGH or LOW	Not Used – but must tie off
CHIP_ADDR	Tie all bits LOW	Serial interface ID bits not used
SCL	Tie HIGH	Not using serial interface
PADDR	----	Used for parallel interface
PDATA	----	Used for parallel interface
SDA	Tie HIGH	Not using serial interface
BOUT	UNCONNECTED	Not Used
ACLR	Tie HIGH	No external pointer manipulation in this example
BCLR	Tie HIGH	Not used in this example
ASET	Tie HIGH	Not used in this example
BSET	Tie HIGH	Not used in this example
AMARK	Tie HIGH	Not used in this example
BMARK	Tie HIGH	Not used in this example
RSET	Tie HIGH	Not used in this example
RCLR	Tie HIGH	Not used in this example
AWEN	Tie LOW	This example expects continuous input data stream
BWEN	Tie to AWEN	In single channel mode, always tie to AWEN
AIEN	Tie LOW	Always writing to memory
BIEN	Tie LOW	Always writing to memory
AREN	Tie LOW	This example expects continuous input data stream
BREN	Tie to AREN	In single channel mode, always tie to AREN
PROGRAM	Tie HIGH	This example uses parallel interface
LOAD	----	LOW at start of operation, bring HIGH after configuration
RESET	----	LOW for >=1 cycles prior to configuration (while LOAD is LOW)
AOE	Tie LOW	This example never disables AOUT
BOE	Tie HIGH	BOUT is not used
CSB	----	Used for parallel interface
WEB	----	Used for parallel interface
REB	----	Used for parallel interface

Configuration Register Address	Data[7:0]	Description
2	00	ALATENCY[23:16]
3	DF	ALATENCY[15:9]
4	04	ALATENCY[7:0]
8	80	Single Channel Shift Register, 10bit data word