# Video Synchronization using TRS Data
# LF3312 - Application Note

## OVERVIEW

Timing Reference Signals (TRS) embedded in the input video stream can be detected and used to SET, CLR or MARK the Write pointer. In addition to manipulating the write pointer, the embedded F, V, and H bits from the input data can be output on the external Flag pins in various combinations.

Similarly, the TRS data that is read out of the memory also passed through TRS detector circuit, which analyzes this data and extracts the F, V, and H bits. These TRS timing bits, which are still embedded in the output data, can be output on the external Flag pins in various combinations.

### Using embedded TRS timing to Reset/Clear the Write Pointer

When using the TRS data, the LF3312 should be placed in one of the two FIFO modes: single-channel FIFO mode (Register 8[2:0]=011) or dual-channel FIFO mode (Register 8[2:0]=111)

The 'F' bit within embedded TRS video data can be used to RESET the Write pointer on frame of field boundaries (Register 9 [7:5]=110 resets pointer on frame boundaries, Register 9 [7:5]=111 resets pointer on field boundaries). For frame-based resets, the Write pointer is reset by the EAV that exhibits an F bit that is LOW, where the previous EAV exhibited an F bit that was HIGH. This EAV sequence is saved in its entirety in the first 4 locations of memory; addresses 0, 1, 2, and 3.

In order to trigger the memory to reading the frame/field of video just written to memory, starting from address 0, we must issue an RCLR signal. Upon bringing RCLR LOW (again, this read pointer reset can be level or edge triggered), the Read pointer is reset. In all FIFO modes, it takes 9 AREN-enabled rising edges of RCLK for the contents of address 0 to arrive on AOUT when an RCLR is issued.

### Using embedded TRS timing to Set/Jump the Write Pointer to a Predetermined Address

The 'F' bit within embedded TRS video data can also be used to SET the Write pointer (Register 9 [7:5]=100 sets pointer on frame boundaries, Register 9 [7:5]=101 sets pointer on field boundaries). For frame-based sets, the Write pointer can be set by the EAV that exhibits an F bit that is LOW, where the previous EAV exhibited an F bit that was HIGH. This EAV sequence is saved in its entirety beginning with address N. Address N can come from the pre-loaded ALAT register (using Registers 2,3, & 4 – and setting BSET LOW) or from the BIN/BOUT ports (setting BSETB HIGH).

In order to trigger the memory into reading the frame/field of video just written to memory, starting from address N, we must issue an RSET signal. Upon bringing RSET LOW (again, this read pointer reset can be level or edge triggered), the Read pointer is set to predefined address N. Again, address N can come from the pre-loaded BLAT register (using Registers 5,6, & 7 – and setting BSET LOW and BCLR LOW) or from the BIN/BOUT ports (setting BSET LOW and BCLR HIGH). In all modes, it takes 14 AREN-enabled rising edges of RCLK (including the edge to latch a LOW on RSET) for the contents of address N to arrive on AOUT when a RSET is issued.

## Displaying TRS Timing Bits on External Pins

TRS timing bits can be displayed on the A and/or B flag output pins. The F, V, and H bits can be extracted directly from the input data stream or from the buffered output data stream.

When the LF3312 is in a single channel mode, Register B[3:0] controls which TRS bits are mapped to which output flag pin. In dual channel modes, Register B[3:0] controls Channel A's TRS bit mapping, and Register B[7:4] controls Channel B TRS bit mapping.

| 4TH Word of the EAV / SAV Code (passed to AIN[11:0] or BIN[11:0] | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Word Width** | **Bit11** | **Bit10** | **Bit9** | **Bit8** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| **8 bit** | 1 | F | V | H | X | X | X | X | ---- | ---- | ---- | ---- |
| **10 bit** | 1 | F | V | H | X | X | X | X | X | X | ---- | ---- |
| **12 bit** | 1 | F | V | H | X | X | X | X | X | X | X | X |

## APPLICATION: FRAME-BASED SYNCRHONIZATION OF VIDEO USING EMBEDDED TRS

In the following application, the LF3312 in single-channel FIFO mode synchronizes a video stream to a Master Frame sync signal using the same clock frequency but different timing. Both the external source and master timing domains reference address zero within the memory as the start of the frame.

The Write and Read clocks should be tied to the external video clock and master/system clock respectively.

The embedded TRS data in the video resets the Write pointer on frame boundaries (on the falling edge of the F-bit).

In addition to synchronizing the data, the LF3312 displays the TRS F, V, and H bits from the synchronized video on the APE, APF, and ACOLLIDE pins respectively for monitoring purposes or for timing reference further down the data path.

The only control pin that is required to actively toggle is the RCLR pin, which should be tied to the system/master F-sync. Upon indicating that a new frame is to begin on the system/master domain, its F-sync signal will go LOW – clearing the Read pointer. In all FIFO modes, it takes 9 AREN-enabled rising edges of RCLK for the contents of address 0 to arrive on AOUT, the first sample of the new frame.

The timing of issuing the RCLR "frame/field sync" signal is referenced to RCLK, the system/master video clock.

| PIN | INITIALIZE | DESCRIPTION |
|---|---|---|
| AWCLK | ---- | Connect to external video source clock |
| BWCLK | Tie to AWCLK | Tied to AWCLK |
| RCLK | ---- | Connect to master video clock |
| AIN | ---- | Connect to external video data source |
| BIN | Tie HIGH or LOW | Not Used – but must tie off |
| CHIP_ADDR | Tie all bits LOW | Serial interface chip ID not used |
| SCL | Tie HIGH | Not using serial interface |
| PADDR | ---- | Used for parallel interface |
| PDATA | ---- | Used for parallel interface |
| SDA | Tie HIGH | Not using serial interface |
| BOUT | UNCONNECTED | Not Used |
| ACLR | Tie HIGH | Not used in this example |
| BCLR | Tie HIGH | Not used in this example |
| ASET | Tie HIGH | Not used in this example |
| BSET | Tie HIGH | Not used in this example |
| AMARK | Tie HIGH | Not used in this example |
| BMARK | Tie HIGH | Not used in this example |
| RSET | Tie HIGH | Not used in this example |
| RCLR | ---- | Connect to master F-sync |
| AWEN | Tie LOW | This example expects continuous input data stream |
| BWEN | Tie to AWEN | In single channel mode, always tie to AWEN |
| AIEN | Tie LOW | Always writing to memory |
| BIEN | Tie LOW | Always writing to memory |
| AREN | Tie LOW | This example expects continuous input data stream |
| BREN | Tie to AREN | In single channel mode, always tie to AREN |
| PROGRAM | Tie HIGH | This example uses parallel interface |
| LOAD | ---- | LOW at start of operation, bring HIGH after configuration |
| RESET | ---- | LOW for >=1 cycles prior to configuration (while LOAD is LOW) |
| AOE | Tie LOW | This example never disables AOUT |
| BOE | Tie HIGH | BOUT is not used |
| CSB | ---- | Used for parallel interface |
| WEB | ---- | Used for parallel interface |
| REB | ---- | Used for parallel interface |

| Configuration Register Address | Data[7:0] | Description |
|---|---|---|
| 8 | 83 | Single Channel FIFO Mode, 10bit data word |
| 9 | C0 | F-bit of TRS EAV clears write pointer, use falling edge of F-bit |
| B | 03 | Output F,V,H bits of AOUT data on APE, APF, ACOLLIDE pins |