



Parallel Interface

Using the parallel interface on the LF3324 is complicated slightly by the fact that the LF3324 is comprised of two die each with its own parallel interface. The two die share a common PDATA and PADDR but have their own Chip Enable (PCE0 and PCE1). For Configuration Registers 0 through B, these two die must be programmed identically via the desired interface (parallel or serial). The one exception is Register C. Register C defines each die in a depth expansion chain. Since the two die within the LF3324 expand the depth by 2x, each die must be programmed uniquely. Die 0 is considered "Die 1 of 2" and Die 1 is considered "Die 2 of 2". For this reason, two 'Chip Enable' pins are provided: PCE0 and PCE1 for Die 0 and Die 1 respectively.

The LF3324 datasheet defines a simple sequence for writing configuration registers using the parallel interface. This sequence is called "Reading and Writing Configuration Registers with PRE held LOW". This is by far the simplest approach to using the parallel interface.

Two parallel interface sequences are defined to simplify the programming of the LF3324:

- Writing to Addresses 0 through B
- Writing to Address C

Writing to Registers 0 through B

Both of the LF3324's die can be written to simultaneously. Since both dies' configuration registers should be written with identical data, we can .

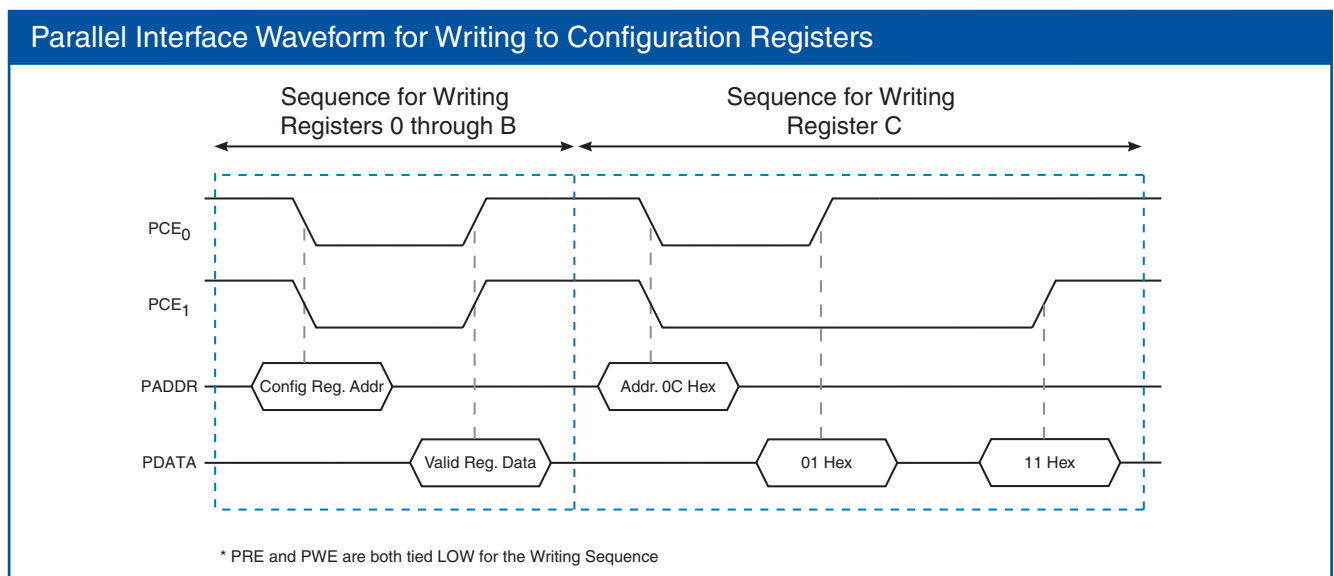
****NOTE:** not all of these registers are required to be written - only pertinent registers need to be addressed.

Writing to Register C

Unique data must be written to each die's Register C address. Register C in Die 0 should be written with 01 Hex. Register C in Die 1 should be written with 011 Hex.

****NOTE:** Register C on both dies **MUST BE WRITTEN**.

The waveform below uses this method and outlines two simple sequences for writing configuration registers.





Serial Interface

Similar to the parallel interface, the serial interface on the LF3324 is complicated slightly by the fact that the LF3324 is comprised of two die each with their own serial interfaces. The two die share a common SDA and SCL but have their own Chip ID codes. The I2C interface calls for a 7bit unique identification code used to differentiate each component (or in our case - each die) in a system. Each LF3324 effectively takes up two unique 7bit ID codes on the I2C shared bus.

The LF3324 has an external 6bit 'Chip ID' port that defines its two unique die identities on the shared I2C bus. Inside, Die 0 appends a zero (0) suffix to the LF3324 6bit Chip ID to make its unique 7bit code. Die 1 appends a one (1) suffix to the LF3324 6bit Chip ID to make its unique 7bit code.

The table below illustrates an example of the two unique I2C addresses required per LF3324.

I2C Identification Code Example										
ID Code	Code Bits (MSB - LSB)								Description	
6bit Chip ID	1	0	1	1	1	0	0			6bit Chip ID on External pins
7bit Die 0 Addr.	1	0	1	1	1	0	0	0		7bit unique Die 0 I2C Address
7bit Die 1 Addr.	1	0	1	1	1	0	0	1		7bit unique Die 1 I2C Address

