

RGB to YCbCR

Full Range 10-Bit RGB to 10-Bit Multiplexed (4:2:2) CCIR-601 YCbCr
(Output Cb/Cr Multiplexed onto one channel)

OVERVIEW

The LF3370 Format Converter is a High Performance Video Processing Engine that has been designed to perform a variety of Format Conversions. The following discussion is meant to give clear and precise guidance in order to configure the LF3370 to perform an RGB to YcbCr format conversion.

The LF3370 performs this conversion by employing the use of a Matrix Multiplier function, Halfband Decimation Filters, and output bias (offset) adders as seen in Figure 2 of the datasheet.

The RGB input data goes through the Matrix Multiplier and the intermediate Y', Cb', and Cr' channels emerge at its output. The Cb' and Cr' words are fed into the Halfband Decimator Filters, whereby their resulting data rate is halved. Since the Y' channel data rate does not need to be reduced, it simply passes through a programmable delay that is matched to the latency of the Halfband Filter. The offsets required on the desired YcbCr data are applied to the intermediate 4:2:2 data at the Output Bias Adders. The Output Multiplexer synchronizes and alternates Cb/Cr data on one output channel.

Input/Output Formats

Table 1 outlines the Input and Output formats and their inclusive ranges for this application.
(Alternative Input/Output Word Size Applications Can be Derived From This Application Note)

Table 1			
Color Space	Range	Format	Word Size
RGB	0-1023	Unsigned	10-Bits
Y' (internal)	0-876	Unsigned	10-Bits
Cb' (internal)	+ -448	Signed	10-Bits
Cr' (internal)	+ -448	Signed	10-Bits
Y	64-940	Unsigned	10-Bits
Cb	64-960	Unsigned	10-Bits
Cr	64-960	Unsigned	10-Bits

Input Data Word Alignment

The 10-bit R, G, and B input words should be aligned on the A, B, and C input ports respectively, in a manner that preserves their non-signed format. Table 2 illustrates the suggested alignment of the Red input word. The same alignment is true for the Green and Blue input words.

Table 2													
Input Pin	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
Input Data	GND	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	GND	GND

Matrix Multiply

At the heart of the Color-Space Conversion is the Matrix-Multiply calculation. The Multiplier coefficients depend on two variables: the range of the Y/CbCr output word and the range of the RGB input word.

(Note: the offsets of 64 or 512 indicated in these equations are accomplished in a separate 'bias adder' function near the output)

The RGB to YcbCr Matrix-Multiply And Offset Equations are as follows:

$$Y = (Y \text{ Range}/\text{RGB Range})(0.299R + 0.587G + 0.114B) + 64$$

$$Cb = (\text{Cb Range}/\text{RGB Range})(-0.1687R - 0.3313G + 0.5B) + 512$$

$$Cr = (\text{Cr Range}/\text{RGB Range})(0.5R - 0.4187G - 0.0813B) + 512$$

Since the Y Output Range is 876 (940-64), the Cb/Cr Output Range is 896 (960-64), and the RGB Input Range is 1023 (1023-0), the equation for this application becomes:

$$Y = (0.256R + 0.50267G + 0.0976B) + 64$$

$$Cb = (-0.14779R + -0.2902G + 0.4379B) + 512$$

$$Cr = (0.4379R + -0.3667G + -0.0712B) + 512$$

The 13-bit coefficients, their bit weighting with respect to the RGB data, and the configuration of the Round/Select/Limit circuit is illustrated in Table 4. A detailed description of the Coefficient and RSL loading method appears later in this document.

Decimation From 4:4:4 to 4:2:2

In this application, the LF3370 uses its 2 Halfband Filters to reduce the data rate (Decimate) the intermediate Cb' and Cr' data by 2. The input 4:4:4 data becomes 4:2:2 data. To this end, the 'Functional Arrangement' should be configured such that the Matrix Multiplier feeds data to the Halfband Filter (see Figure 2 of the datasheet).

The synchronous pin SYNCB must be toggled from HIGH to LOW and held there in order to initialize the Halfband Decimation function and Output Multiplexer. This must be done before valid data is streamed through the part.

The bit weighting of the Halfband output and the configuration of the Round/Select/Limit circuit that conditions its output is illustrated in Table 4. A detailed description of the RSL loading method appears later in this document.

Output Offset Adjustment

The LF3370 handles the offset addition in the conversion equations by using the 'Output Bias' adders. Half LSB Round bits were added to the output offset words in order to round the 10-bit output word (See Table 4). The output bias adder configuration and a detailed description of the loading method appear near the end of this document.

Output Cb/Cr Multiplexing

The Output Multiplexer interleaves alternating Cb and Cr data onto the X12-0 output port. A LOW on the Least Significant bit of the Y12-0 output pins (Y0) indicates that a Cb sample is present on the X12-0 output pins (See Figure 6 of the datasheet). This 'Output Sync' pin can be used to externally de-multiplex the Cb/Cr data.

As additional information, the next rising of CLK, or any odd number of rising CLK edges after latching a HIGH to LOW event on SYNCB will produce a Cb sample on the X12-0 output pins.

Output Word Alignment

Table 3 illustrates the alignment of the 10-bit Y output word on the W output port. (Please note that the same alignment is true for the alternating Cb and Cr output words on the X output port)

Table 3													
Output Pin	W12	W11	W10	W09	W08	W07	W06	W05	W04	W03	W02	W01	W00
Output Data	NC	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	NC	NC

Configuration Register Loading

The following tables refer to the addresses and data that need to be loaded into the LF interface in order to configure the part to perform this RGB to YcbCr Conversion. Loading the entire sequence of address and data words from these tables into the CF12-0 bus will achieve the desired configuration. (For more information on the Lfinterface please refer to the LF3370 data sheet)

Note: For this application we assume that the Blanking Feature, Core Bypass Feature and the Key Channel are not being used. (If these features are required, please refer to the LF3370 data sheet for their descriptions)

Address/Data	Description
0000	Matrix Coefficient Address 0
041B	0.256 = Bank 0
080A	0.50267 = Bank 1
018F	0.0976 = Bank 2
1DA3	-0.14779 = Bank 3
1B5C	-0.2902 = Bank 4
0701	0.4379 = Bank 5
0701	0.4379 = Bank 6
1A22	-0.3667 = Bank 7
1EDD	-0.0712 = Bank 8
0000	0.0 = Bank 9

Address/Data	Description
0200	Input/Output Format and Functional Arrangement
015B	3 Ch In/2 Ch. Out, Matrix to Halfband, Decimation Enabled
Address/Data	Description
0201	Gamma LUT, Blanking, and Bias Enables
0800	Disable LUT, No Blanking, Enable Output Offset Adjustment
Address/Data	Description
0203	Y Channel Filter Bypass Delay
0021	$35-2 = 33$
Address/Data	Description
0900	Output Bias For Y Channel
0102	Output Bias = 64.5
0A00	Output Bias For Cb Channel
0802	Output Bias = 512.5
0B00	Output Bias For Cr Channel
0802	Output Bias = 512.5
Address/Data	Description
0E00	Matrix RSL For Y Channel
0008	LSB Rounding
0000	Select Window = 0
0DB0	Upper Limit = +876
0000	Lower Limit = 0
Address/Data	Description
0F00	Matrix RSL For Cb Channel
0008	LSB Rounding
0000	Select Window = 0
0700	Upper Limit = +448
1900	Lower Limit = -448
Address/Data	Description
1000	Matrix RSL For Cr Channel
0008	LSB Rounding
0000	Select Window = 0
0700	Upper Limit = +448
1900	Lower Limit = -448
Address/Data	Description
1200	Halfband Filter RSL For Cb Channel
0040	LSB Rounding
0300	Select Window = 3
0700	Upper Limit = +448
1900	Lower Limit = -448
Address/Data	Description
1300	Halfband Filter RSL For Cr Channel
0040	LSB Rounding
0300	Select Window = 3
0700	Upper Limit = +448
1900	Lower Limit = -448

Table 4. 10 Bit RGB to 10 Bit YCbCr CCIR-601 Format Conversion																																							
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12											
INPUT PINS						A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0																					
						0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0																					
INPUT PINS						B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0																					
						0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	0	0																					
INPUT PINS						C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0																					
						0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0																					
MATRIX MULT INPUT WORDS																																							
						R'	R'	R'	R'	R'	R'	R'	R'	R'	R'	R'	R'	R'	R'																				
						G'	G'	G'	G'	G'	G'	G'	G'	G'	G'	G'	G'	G'	G'	G'																			
						B'	B'	B'	B'	B'	B'	B'	B'	B'	B'	B'	B'	B'	B'	B'																			
COEFFICIENT FORMAT																																							
																	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0										
Y' MATRIX CH. OUTPUT																																							
						Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'										
R						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
S																SEL=00																							
UL						0	1	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
LL						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
Cb'/Cr' MATRIX CH. OUTPUT																																							
						Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'									
R						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									
S																SEL=00																							
UL						0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
LL						1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
Cb'/Cr' HALFBAND OUTPUT																																							
						Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'								
R						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
S																SEL=03																							
UL						0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
LL						1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
OUTPUT BIAS A						Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'	Y'								
						0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
OUTPUT BIAS B						Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'	Cb'							
						0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
OUTPUT BIAS C						Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'	Cr'						
						0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
OUTPUT PINS						W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W0																					
						NC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	NC	NC	Y OUTPUT WORD																			
OUTPUT PINS						X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0																					
						NC	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	NC	NC	CB OUTPUT WORD																				
OUTPUT PINS						Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0																					
						NC	CR	CR	CR	CR	CR	CR	CR	CR	CR	CR	CR	NC	NC	CR OUTPUT WORD																			