LOGIC
DEVICES INCORPORATED

LF3320
Polyphase 1:M Upsampling

1:M POLYPHASE UPSAMPLING

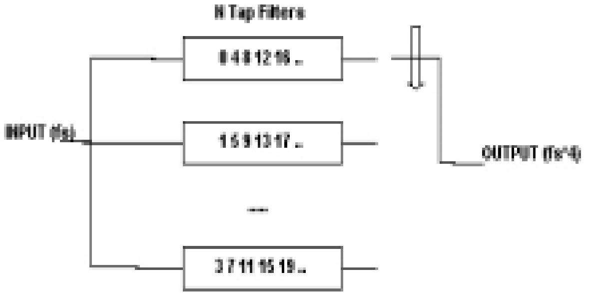
The objective of upsampling is to increase a signal's sample rate. 1:M Upsampling is sometimes accomplished by placing M-1 zeros between input samples, and then filtering out the spectral copies. This 2-step process can be costly and inefficient. Polyphase upsampling allows us to effectively zero-fill the input data AND bandlimit the upsampled signal efficiently within one LF3320. Note: 2 separate polyphase filters can be implemented within one LF3320 (in Dual Filter Mode).

When upsampling, although we have a new higher sample rate Fs, the original baseband spectral copies are still spaced at the old sample rate. These spectral copies do not belong in the new upsampled spectrum and must be filtered out. This necessitates a Bandlimiting filter with a cutoff frequency of fs/(2M). Therefore, 1:2 upsampling requires an fs/4 cutoff. Upsampling of 1:3 requires a fs/6 cutoff, etc. This Bandlimit filter is what we implement when performing polyphase filtering. Figure 2 illustrates the fs/8 filter we used for the 1:4 upsampling example in this note.

The Polyphase technique takes M phases of a relatively large filter coefficient set, and groups them into M separable filters – which are the M phases of the large coefficient set. Each unique filter processes the data in turn. Figure 1 illustrates the filter structure in our 1:4 polyphase implementation.

The separate filters are actually implemented with our single FIR filter. Using multiple coefficient sets, we can make one hardware Filter appear as many more. In fact, the LF3320 has 256 coefficient sets – making it capable of performing upsampling of up to 1:256.

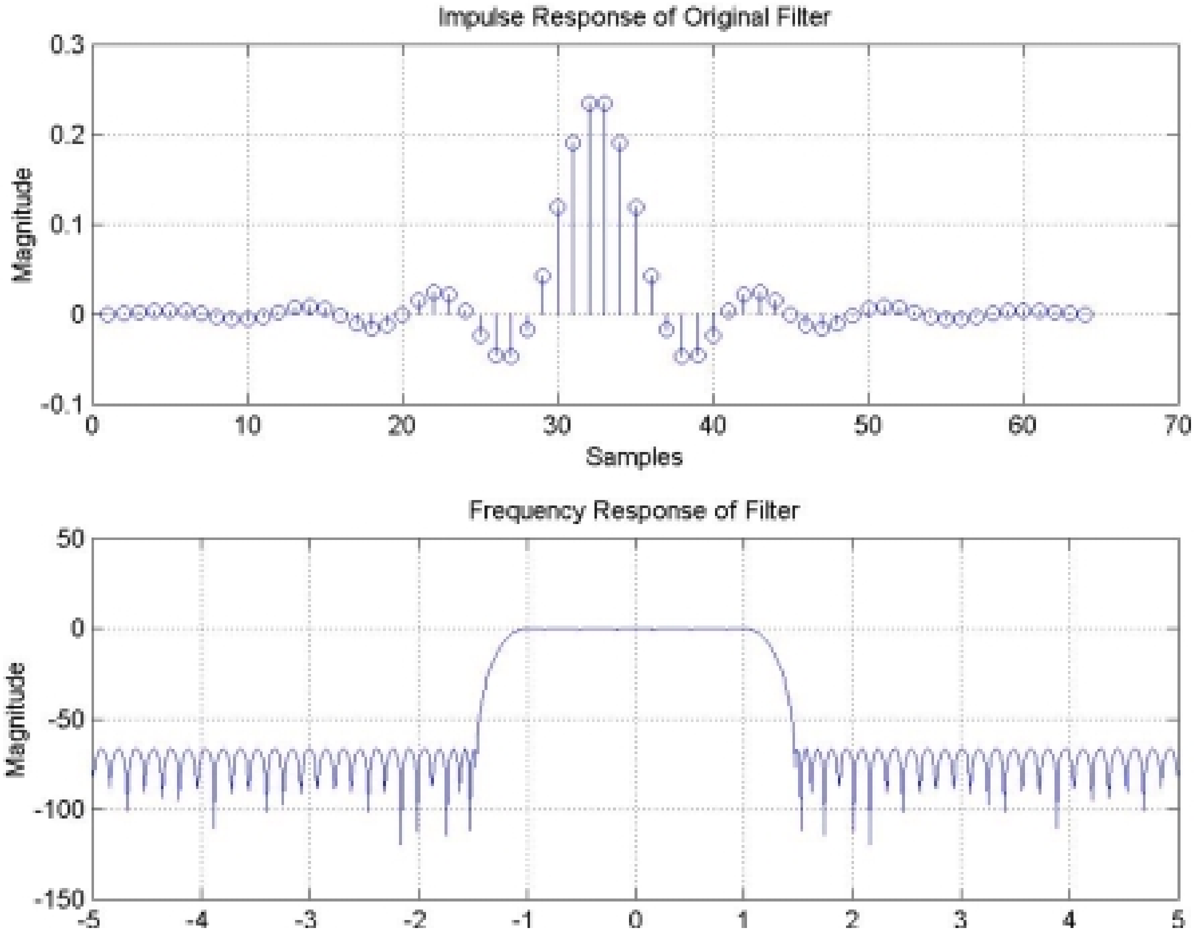
Figure 1. 1:4 Polyphase Implementation



Assuming we use the LF3320 in Single Filter mode to perform a 1:M upsampling filter, we ultimately implement a 16*M tap filter. Note: although the original filter may be symmetric, splitting the upsampling filter coefficients into M filter phases ruins this symmetry. So we only have access to our 16 hardware taps. The value of this 'Single Filter Mode' implementation is in the relatively large filters that we can create.

We based this particular application note on 1:4 Upsampling. Therefore, our LF3320 will accommodate 16*4 = 64taps. We will take these 64 taps and break them into 4 groups (M=4) of 16 taps each. These 4 filter groups are the 4 phases of our original 64tap filter. A paragraph near the end of this discussion describes how we break up the coefficients into their respective phases and storage locations. Table 2 lists the coefficients and their respective addresses.

Figure 2. Upsampling Bandlimit Filter Coefficient Set and Frequency Response



Note: Filter A coefficient banks 0 through 7 receive the first 8 taps of the 16tap filter phase, and Filter B coefficient banks 0 through 7 receive the last 8 taps of the 16tap filter phase.

We load the 4 filter sets into 4 banks of our coefficient storage. Each new data sample is shifted into the filter and held. We then present the 4 phases of the original coefficient set to the input data using coefficient address cycling. The 4 filter results become 4 output data samples. Therefore, for every 1 input data sample, we create 4 output samples. This sequence of shifting data into the part, holding, and cycling through the 4 phases of the original coefficient set continues indefinitely. The timing and toggling sequence of CA (coefficient address), and SHEN (shift enable control) is extremely important. Table 3 illustrates the correct timing sequence for the 1:4 upsample factor. Figure 3 is a waveform diagram that explicitly describes this sequence.

Tables 1 and 2 show appropriate configuration register settings as well as coefficient values and loading sequence for our 1:4 upsampling example.

Bit Weighting and Coefficient Scaling

Since the maximum coefficient value for this upsampling polyphase filter is just less than 0.25, we have scaled the coefficients up by 2^2 to fit as much precision within our 12bit coefficient storage as possible. For example, the coefficient 0.2391 will be represented by the 12bit hex value of 7A7h. So a gain of 2^-2 (shift of 2) must be applied to the filter output data. We will perform this shift later in the RSL section.

1:M upsampling has an inherent gain reduction of M. Therefore our upsampling example requires a gain of 4 (2^2) to restore the signal to its original scaling.

Since there are 11 bits below the radix point in our coefficients, we would typically load an 11 (B hex) into the Select register. It is interesting to note that the required upsampling gain increase of 2^2 and the coefficient scaling 2^-2 cancel each other – and we are left with loading 11(B hex) into Address 400h (Filter A Select Register).

Table 1. Configuration Loading

CFA	ADDRESS	400
	DATA	00B
CFA	ADDRESS	800
	DATA	000
	DATA	000
	DATA	000
	DATA	000
CFA	ADDRESS	C00
	DATA	001
	DATA	0F8
	DATA	0FF
	DATA	007
CFA	ADDRESS	200
	DATA	002
CFA	ADDRESS	201
	DATA	040
CFA	ADDRESS	202
	DATA	002
CFA	ADDRESS	203
	DATA	040
CFA	ADDRESS	204
	DATA	002
CFA	ADDRESS	205
	DATA	000

Table 2. Coefficient Loading

CFA	ADDRESS	000	CFB	ADDRESS	000
	DATA	000		DATA	780
	DATA	022		DATA	F74
	DATA	FD7		DATA	022
	DATA	03D		DATA	002
	DATA	FA7		DATA	FF0
	DATA	07E		DATA	014
	DATA	F46		DATA	FEE
	DATA	15F		DATA	01D
CFA	ADDRESS	001	CFB	ADDRESS	001
	DATA	008		DATA	620
	DATA	01C		DATA	E82
	DATA	FD3		DATA	0B6
	DATA	04D		DATA	FA0
	DATA	F82		DATA	031
	DATA	0CF		DATA	FEA
	DATA	E90		DATA	009
	DATA	3D6		DATA	012
CFA	ADDRESS	002	CFB	ADDRESS	002
	DATA	012		DATA	3D6
	DATA	009		DATA	E90
	DATA	FEA		DATA	0CF
	DATA	031		DATA	F82
	DATA	FA0		DATA	04D
	DATA	0B6		DATA	FD3
	DATA	E82		DATA	01C
	DATA	620		DATA	008
CFA	ADDRESS	003	CFB	ADDRESS	003
	DATA	01D		DATA	15F
	DATA	FEE		DATA	F46
	DATA	014		DATA	07E
	DATA	FF0		DATA	FA7
	DATA	002		DATA	03D
	DATA	022		DATA	FD7
	DATA	F74		DATA	022
	DATA	780		DATA	000

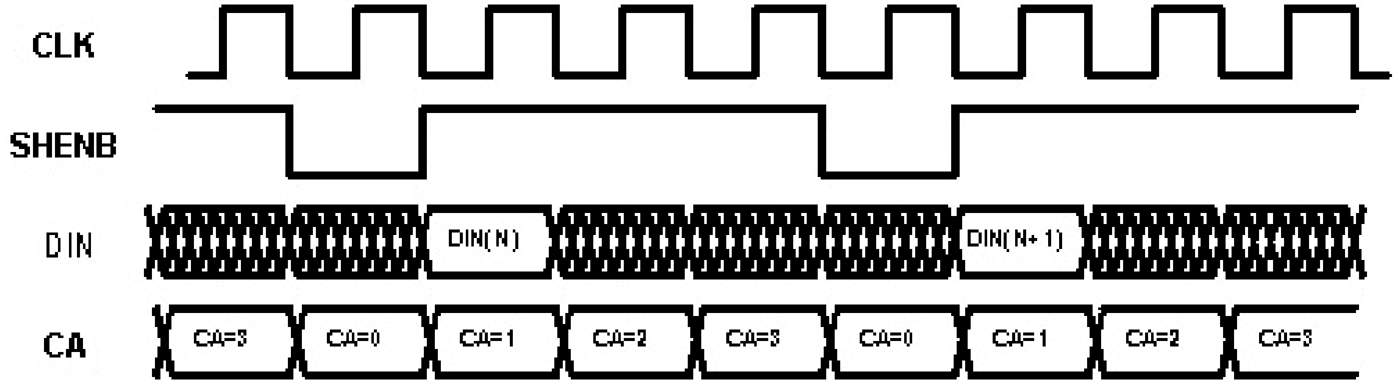
Table 3. Control Sequence

DIN	SHENA/B	TXFRA/B	CA/B	ACCA/B	DOUT
XXX	0	1	0	0	DOUT(n)
VALID	1	1	1	0	DOUT(n+1)
XXX	1	1	2	0	DOUT(n+2)
XXX	1	1	3	0	DOUT(n+3)
XXX	0	1	0	0	DOUT(n+4)
VALID	1	1	1	0	DOUT(n+5)
XXX	1	1	2	0	DOUT(n+6)
XXX	1	1	3	0	DOUT(n+7)
XXX	0	1	0	0	DOUT(n+8)
		.	.	.	.

NOTE: As previously stated, the first phase (coefficients 0, 4, 8, etc. of the original set) are loaded into Address 0 in the coefficient memory. The second phase (coefficients 1, 5, 9, etc. of the original set) are loaded into Address 1 in the coefficient memory. This is done for all 4 phases of the original coefficient set. The coefficient Address (CA) in Table 3 refers to addressing a certain phase of the original coefficient set. For example, CA=3 addresses the final phase of the original set, which are coefficients 3, 7, 11, etc.

NOTE: Tie SHENA/SHENB LOW. Also, tie Filter A and Filter B common control pins together (CAA/CAB, TXFRA/TXFRB, ACCA/ACCB, etc.)

Figure 3. Control Waveforms



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