

# LOGIC Devices Incorporated

*Providing Chip Solutions*



## LOGIC DEVICES INCORPORATED



DEVELOPS AND MARKETS HIGH PERFORMANCE INTEGRATED CIRCUITS THAT ARE UTILIZED IN A WIDE RANGE OF VIDEO AND MEDICAL IMAGE PROCESSING, TELECOMMUNICATIONS, COMPUTING, AND MILITARY APPLICATIONS. LOGIC IS COMMITTED TO PROVIDING ITS CUSTOMERS WITH HIGH PERFORMANCE PRODUCTS THAT OFFER EXCEPTIONAL QUALITY, COMPETITIVE PRICING, RESPONSIVE DELIVERY, AND COMPREHENSIVE TECHNICAL SUPPORT.

LOGIC DEVICES MARKETS ITS PRODUCTS THROUGH DIRECT SALES OFFICES IN NORTH AMERICA AND EUROPE, AND THROUGH A WORLD WIDE NETWORK OF DISTRIBUTORS AND MANUFACTURERS' SALES REPRESENTATIVES. IN 2000, EXPORTS ACCOUNTED FOR 39% OF TOTAL REVENUES.

LOGIC DEVICES WAS FORMED IN 1983 AND IS LISTED ON THE NASDAQ NATIONAL MARKET SYSTEM UNDER THE SYMBOL LOGC. CORPORATE HEADQUARTERS ARE LOCATED IN SUNNYVALE, CALIFORNIA. PRODUCT INFORMATION CAN BE ACCESSED ON THE WORLDWIDE WEB AT [HTTP://WWW.LOGICDEVICES.COM](http://www.logicdevices.com).

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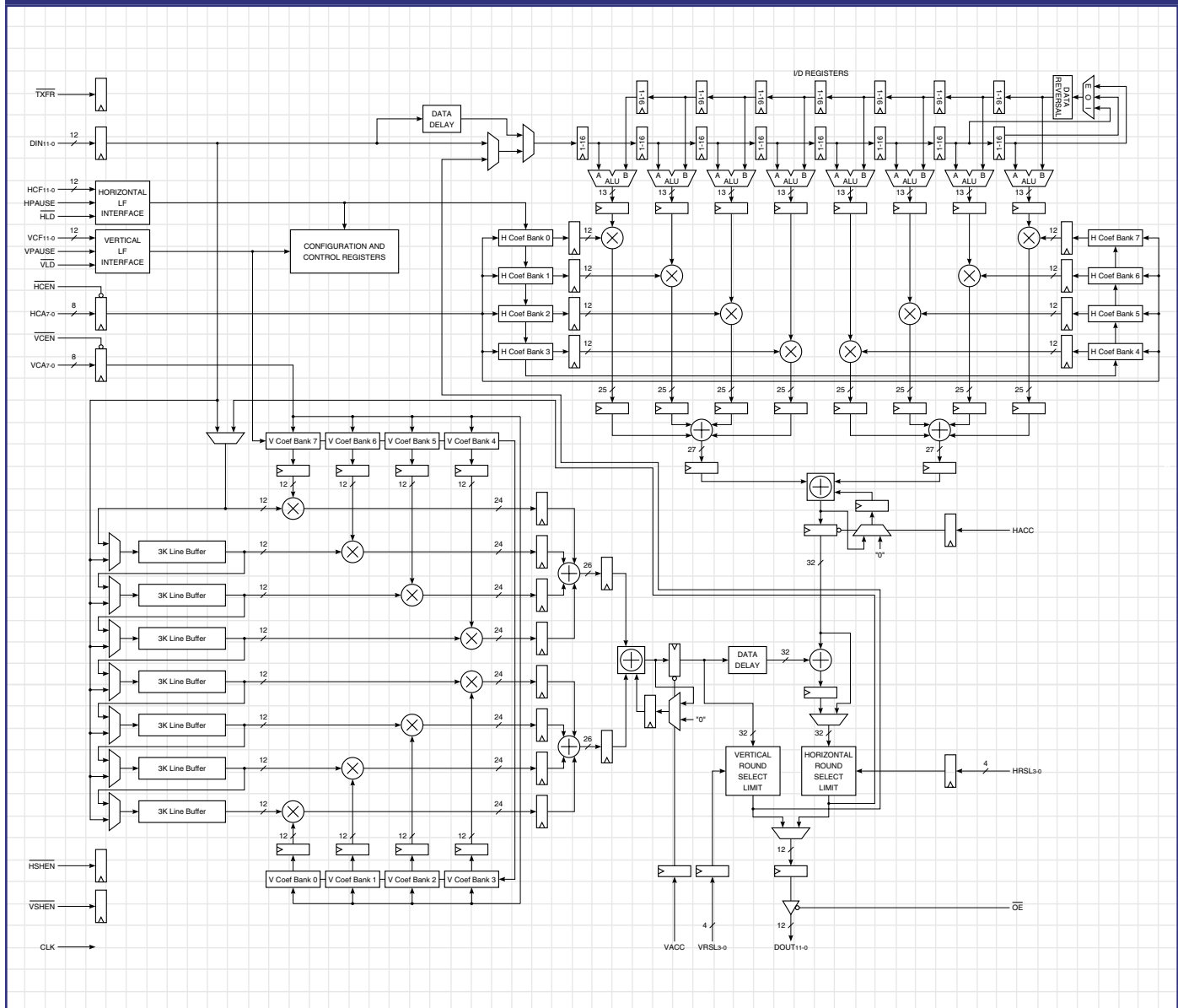
## Features

- ▶ 83 MHz Data Rate
- ▶ Seven 3K x 12-bit, Programmable Two-Mode Line Buffers
- ▶ 16 Horizontal and 8 Vertical Filter Taps
- ▶ 12-bit Data and Coefficients
- ▶ Embedded Memory for 256 Horizontal and Vertical Coefficient Sets
- ▶ Selectable 12-bit Data Output with User-Defined Rounding and Limiting
- ▶ Supports Dimensionally Separate Filtering and Orthogonal Kernels
- ▶ Allows Interleaved Data Streams for Multi-Channel Applications
- ▶ All 4096 Coefficients can be Updated Within 27.7  $\mu$ s
- ▶ Horizontal Filter Supports Decimation Up to 16 x 1 for Increasing Number of Filter Taps
- ▶ 3.3 Volt Power Supply
- ▶ 5 Volt Tolerant I/O
- ▶ 144-pin PQFP Package
- ▶ Industrial Temperature Available

## Applications

- ▶ Microprocessor Control of LF Interface
- ▶ Filtering Interleaved Data
- ▶ Filtering with General 2D Kernels
- ▶ Image Filtering Resampling / Resizing
- ▶ Behavioral Models Available

### LF3310 Functional Block Diagram



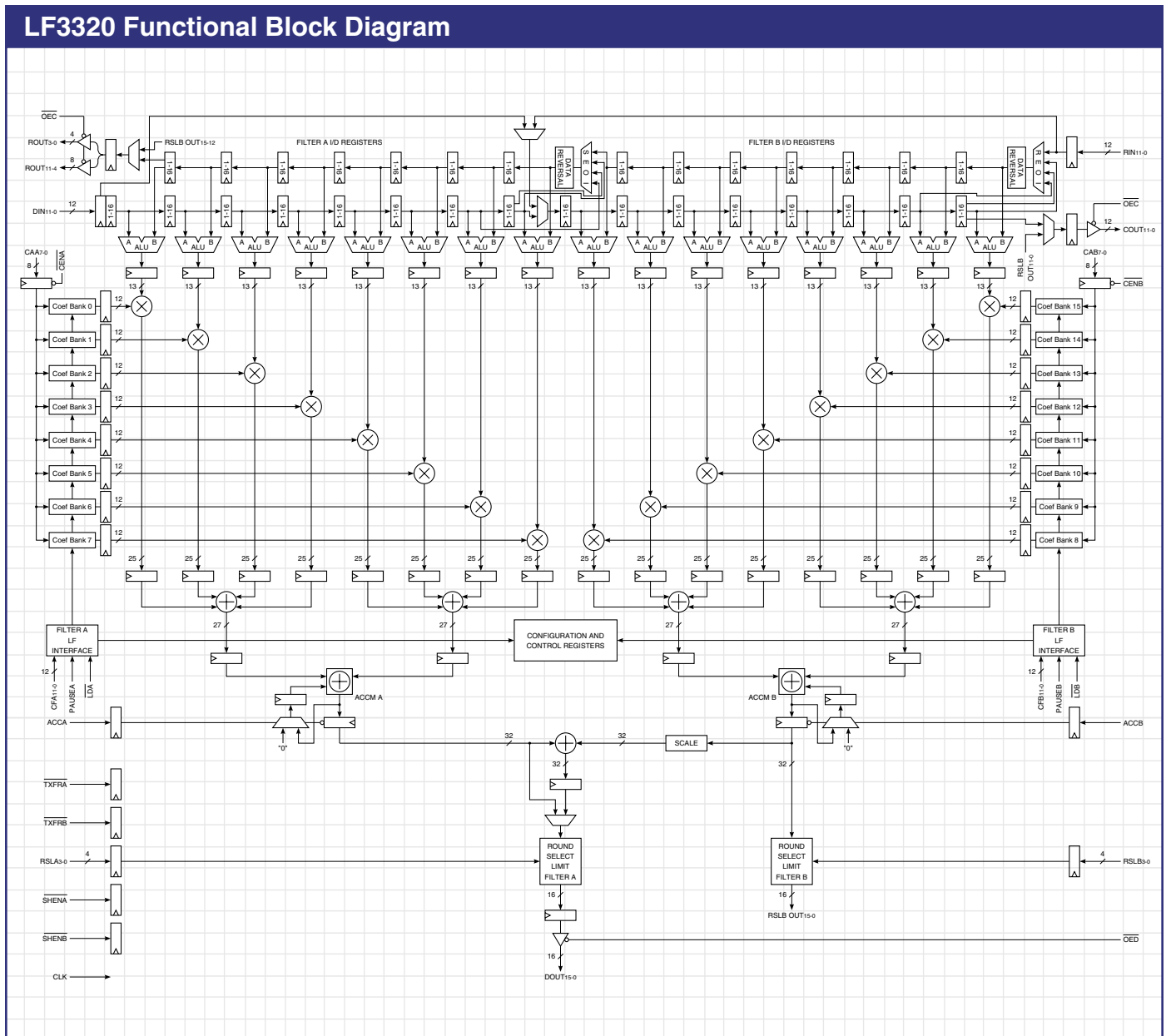
## Features

- ▶ 83 MHz Data Rate
- ▶ 32-Tap Transversal FIR Filter
- ▶ Cascadable for More Filter Taps Using the LF3347
- ▶ Single or Dual Filter Modes
- ▶ 12-bit Data and Coefficients
- ▶ Embedded Memory for 256 Coefficient Sets
- ▶ Selectable 16-bit Data Output with User-Defined Rounding and Limiting

- ▶ Allows Interleaved Data Streams for Multi-Channel Applications
- ▶ Supports Decimation up to 16:1 for up to 512 Filter Taps
- ▶ All 4096 Coefficients can be Updated Within 27.7  $\mu$ s
- ▶ 3.3 Volt Power Supply
- ▶ 5 Volt Tolerant I/O
- ▶ 144-pin PQFP Package
- ▶ Industrial Temperature Available

## Applications

- ▶ Microprocessor Control of LF Interface
- ▶ Filtering Interleaved Data
- ▶ Filtering with General 2D Kernels
- ▶ Image Filtering Resampling / Resizing
- ▶ Behavioral Models Available
- ▶ Discrete Cosine Transform



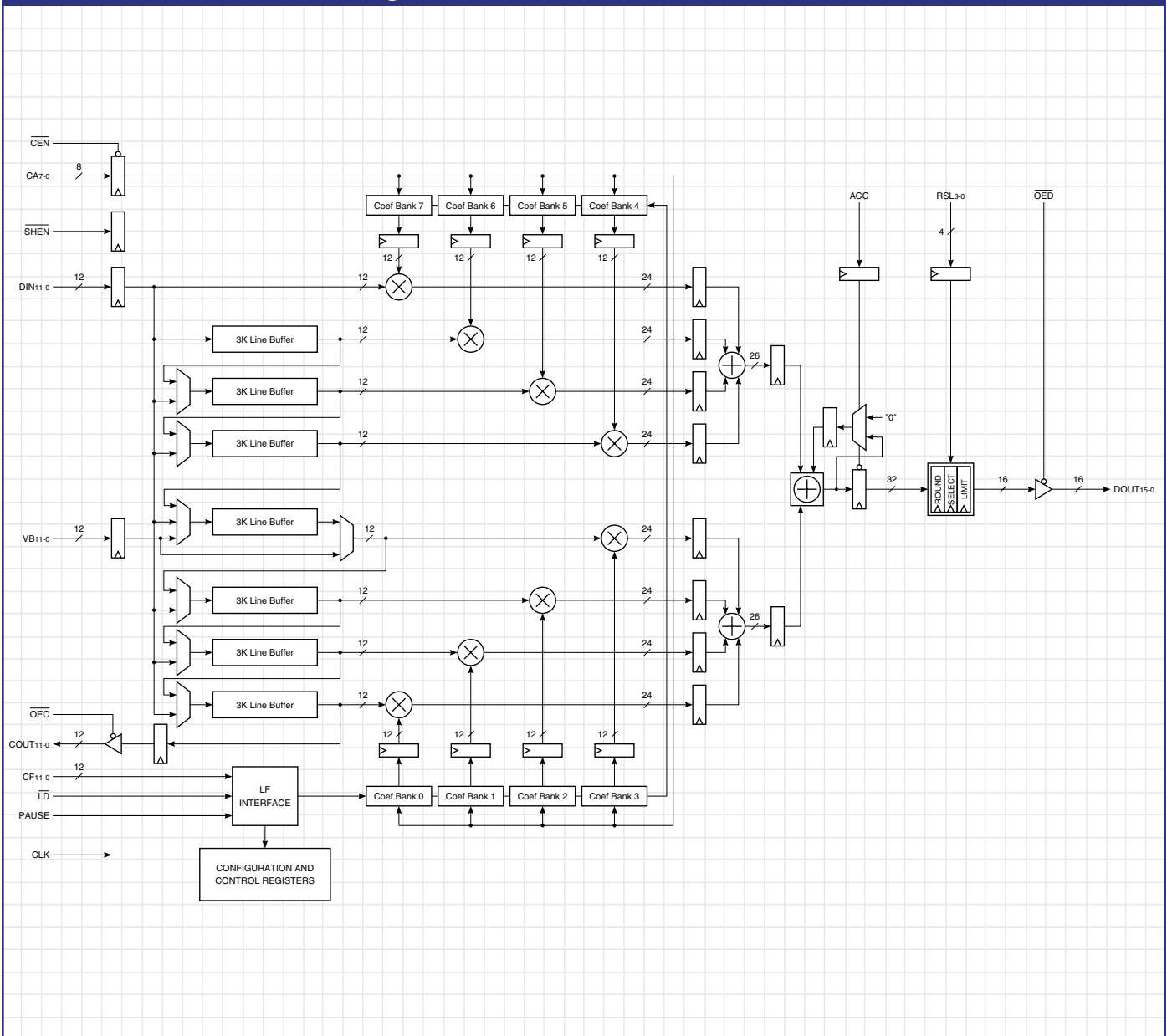
## Features

- ▶ 83 MHz Data Rate
- ▶ Seven 3K x 12-bit, Programmable Two-Mode Line Buffer
- ▶ Cascadable for More Filter Taps Using the LF3347
- ▶ 12-bit Data and Coefficients
- ▶ Embedded Memory for 256 Coefficient Sets
- ▶ Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- ▶ Allows Interleaved Data Streams for Multi-Channel Applications
- ▶ Separate Input Port for Odd and Even Field Filtering
- ▶ All 2048 Coefficients can be Updated Within 27.7  $\mu$ s
- ▶ 3.3 Volt Power Supply
- ▶ 5 Volt Tolerant I/O
- ▶ 100-pin PQFP Package
- ▶ Industrial Temperature Available

## Applications

- ▶ Microprocessor Control of LF Interface
- ▶ Filtering Interleaved Data
- ▶ Filtering with General 2D Kernels
- ▶ Image Filtering Resampling / Resizing
- ▶ Behavioral Models Available

### LF3330 Functional Block Diagram



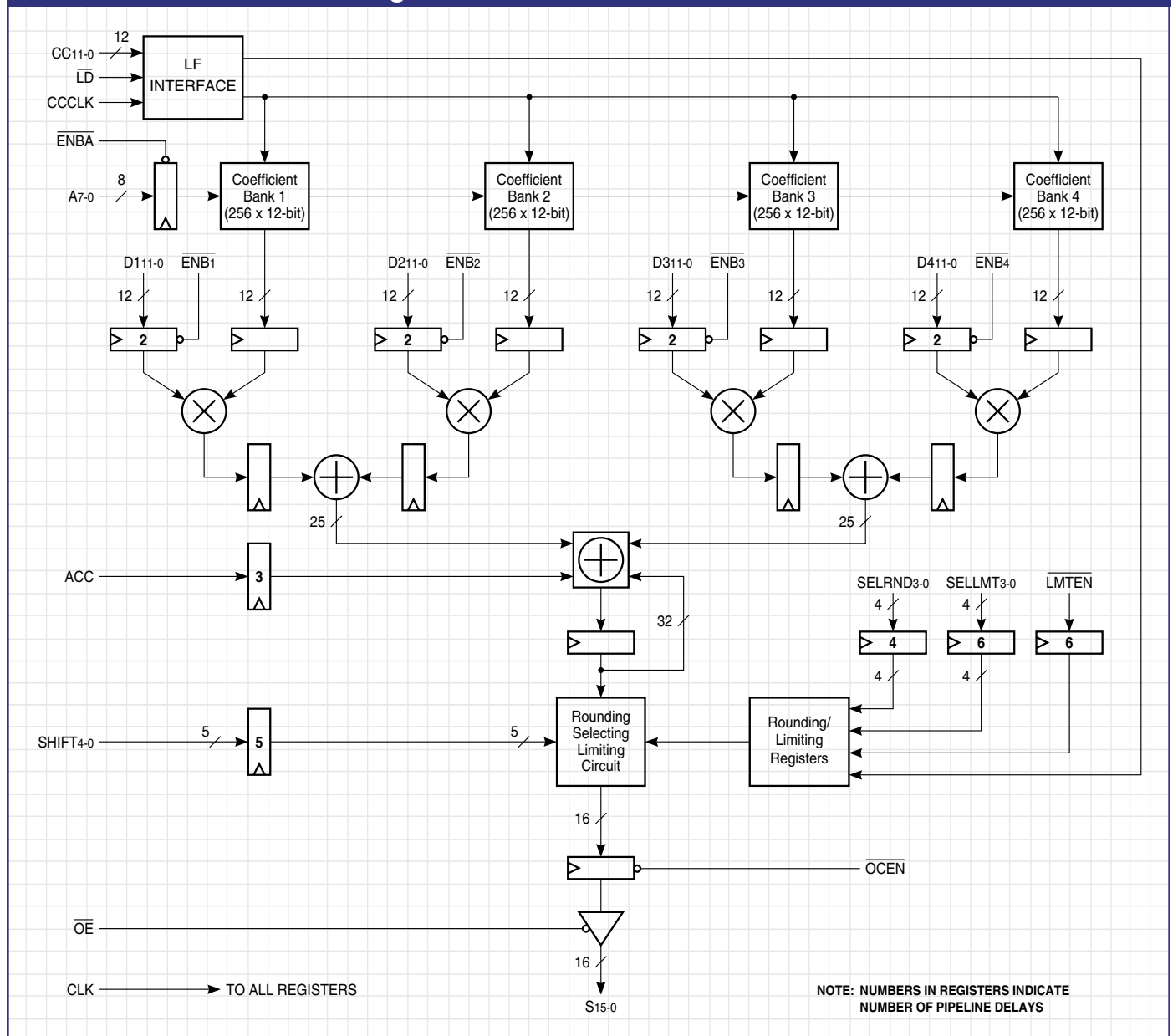
## Features

- ▶ 83 MHz Data Input and Computation Rate
- ▶ Four 12 x 12-bit Multipliers with Individual Data and Coefficient Inputs
- ▶ Four 256 x 12-bit Coefficient Banks
- ▶ 32-bit Accumulator
- ▶ Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- ▶ Two's Complement Operands
- ▶ 3.3 Volt Power Supply
- ▶ 5 Volt Tolerant I/O
- ▶ 120-pin PQFP Package
- ▶ Industrial Temperature Available

## Applications

- ▶ Behavioral Models Available

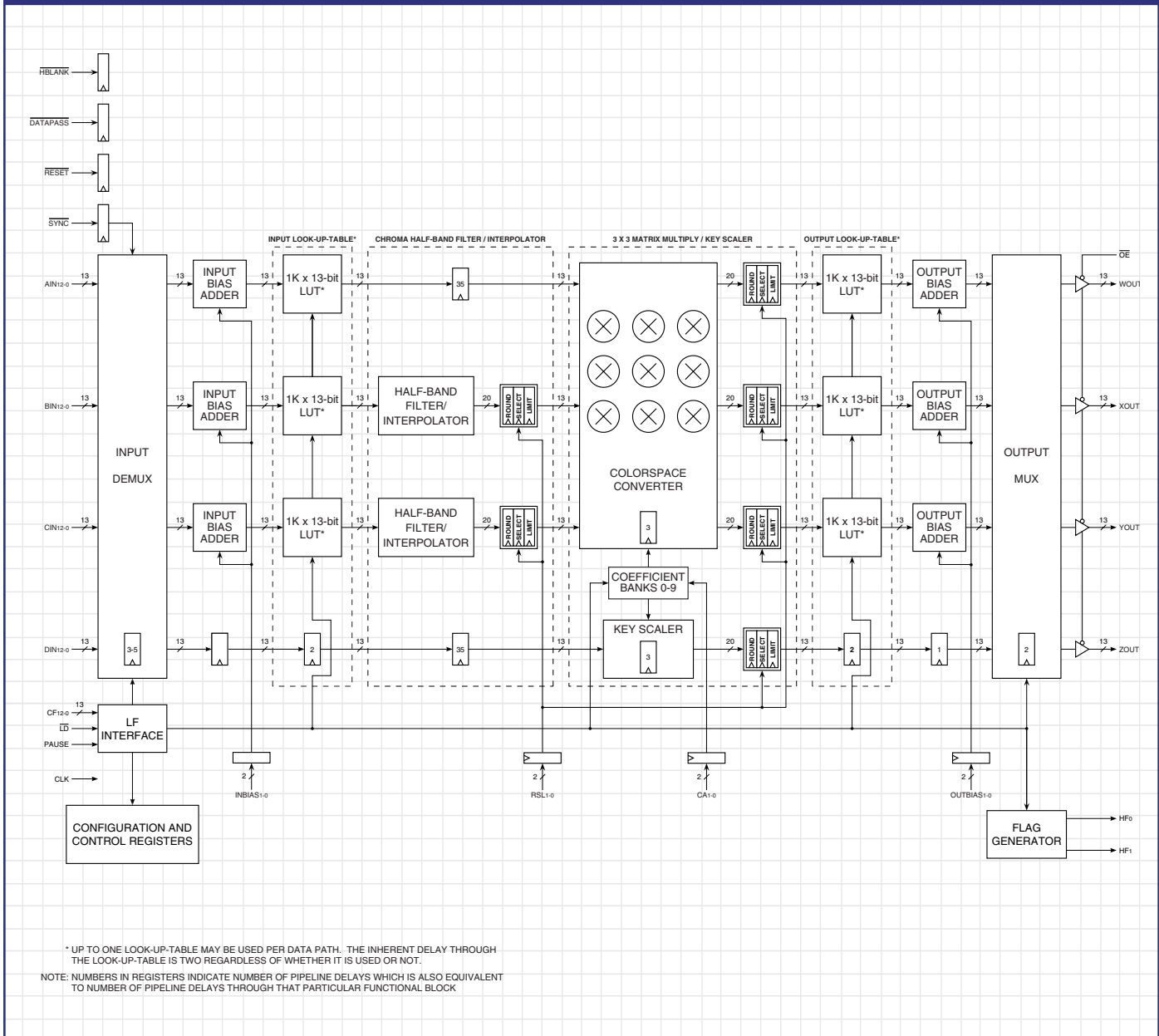
### LF3347 Functional Block Diagram



## Features

- ▶ 83 MHz Data Rate for HDTV Applications
  - ▶ Supports Multiple Video Formats
  - ▶ Multiplexed and Non-multiplexed I/O Data
  - ▶ 13-bit Data Path, Colorspace Converter Coefficients and Key Channel Scaling Coefficients
  - ▶ 3.3 Volt Power Supply
  - ▶ 5 Volt Tolerant I/O
  - ▶ 160-lead PQFP Package
  - ▶ Industrial Temperature Available
- Bi-Directional Conversions:
- 4:2:2:4
  - 4:4:4:4
  - R/G/B/Key
  - Y/U/V/Key
- User-Programmable:
- 3 x 3 Colorspace Converter
  - LUT for Gamma Correction
  - I/O Bias Compensation
  - Bypass Capability

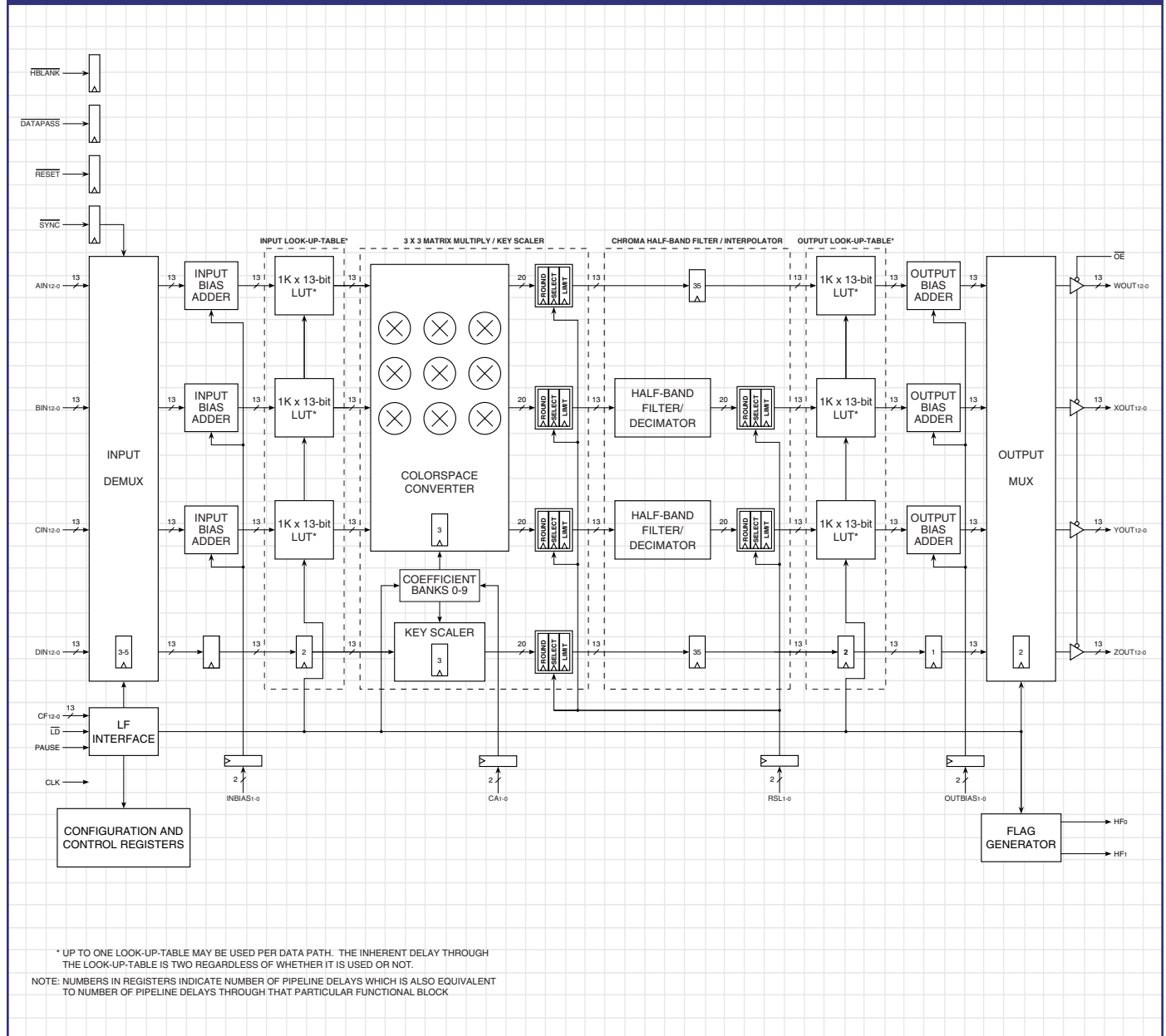
### LF3370 Functional Block Diagram (Half-Band Filter to Colorspace Arrangement)



## Application

- ▶ Microprocessor Control of LF Interface
- ▶ Format Conversion - YCbCr to RGB
- ▶ Format Conversion - RGB to YCbCr
- ▶ Data Bypass
- ▶ Clock and Data Synchronization

### LF3370 Functional Block Diagram (Colorspace to Half-Band Arrangement)



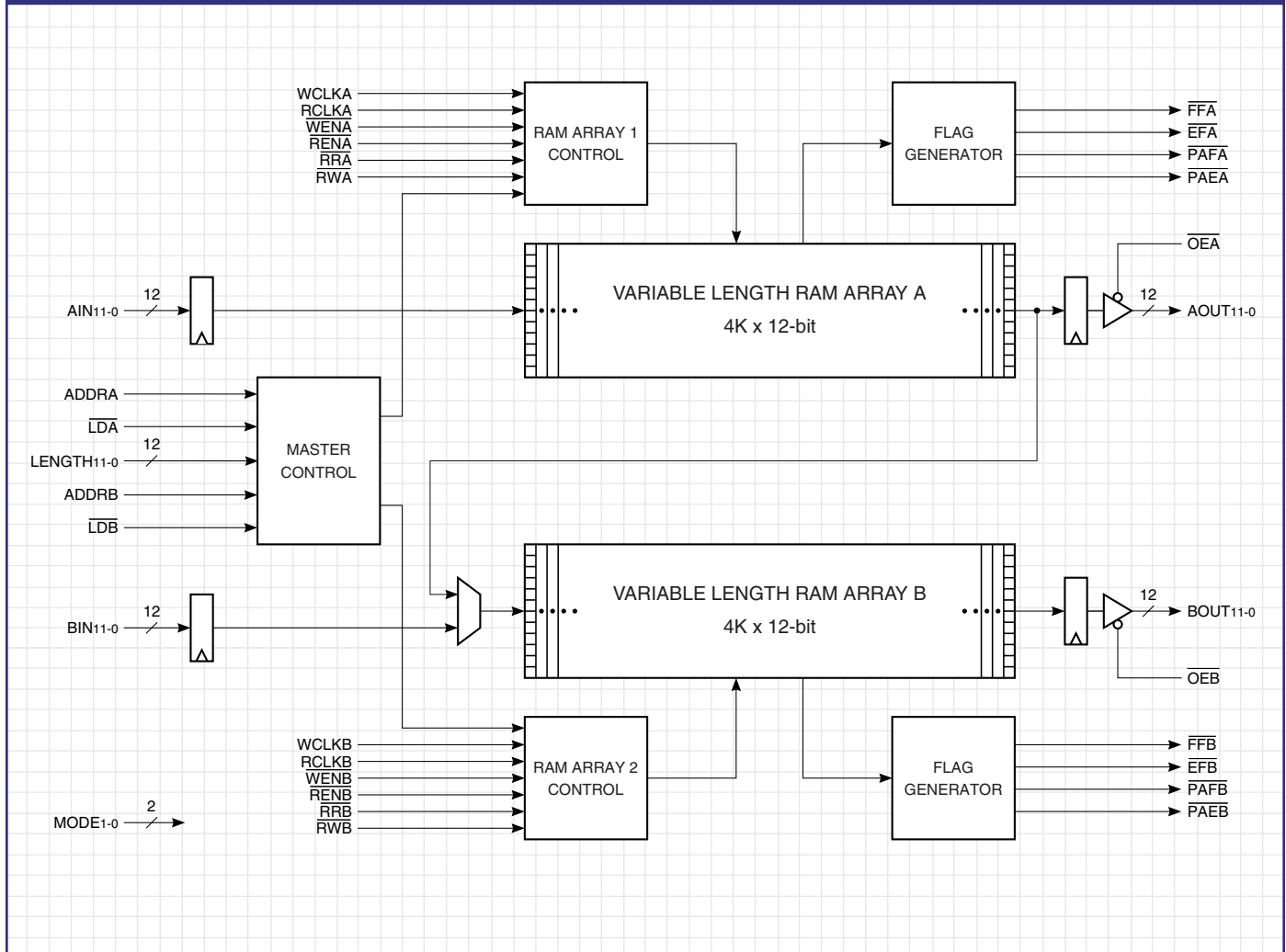
## Features

- ▶ 100 MHz Data Rate for Video and Other High-Speed Applications
- ▶ User-Resettable Read and Write Pointers
- ▶ Dual Modes: Line Buffer or FIFO
- ▶ Organized in the Following Memory Configurations:
  - 4K x 24-bit
  - 8K x 12-bit
  - 4K x 12-bit (2 Channels)
  - 4K x 8-bit (3 Channels)
- ▶ User-Programmable FIFO Flags
- ▶ 3.3 Volt Power Supply
- ▶ 5 Volt Tolerant I/O
- ▶ 100-lead PQFP Package
- ▶ Industrial Temperature Available

## Applications

- ▶ Behavioral Models Available

### LF3304 Functional Block Diagram



## Features

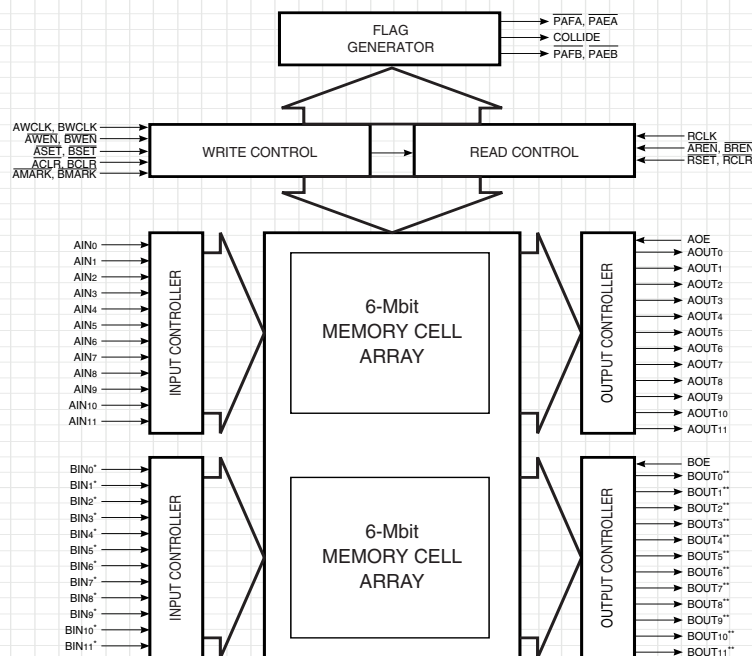
- ▶ 12,441,600-bit Frame Memory
- ▶ Eight Operating Modes:
  - One-Channel Synchronous Shift Register (Single Clock Source)
  - One-Channel Framestore with Sequential Write and Random Access Read
  - One-Channel Framestore with Random Access Write and Sequential Read
  - One-Channel FIFO with Asynchronous I/O
  - Two-Channel Synchronous Shift Register (Single Clock Source)
  - FIFO + Shift Register; Channel B Synchronized to Channel A
  - Shift register + FIFO; Channel A Synchronized to Channel B
  - Two-Channel FIFO; Both Channels Synchronized to External Signal<sup>(a)</sup>
- ▶ Features in the Four Modes with Asynchronous FIFOs:
  - Near-Full/Empty Flags with Programmable Thresholds
- ▶ Features in the Six Purely Sequential (FIFO, shift register) Modes:
  - Up to 100 MHz Continuous Data Throughput Rate
- ▶ Features in the Two Random Access (non-FIFO) Modes:
  - Up to 27 MHz Data Rate
- ▶ LF3312s may be Connected in Parallel for HDTV, multiframe SDTV, etc.
- ▶ Built-in ITUR-656 TRS Detection and Synchronization
- ▶ May be Organized Into the Following Configurations:
  - 1,555,200 x 8-bit (single channel)
  - 1,244,160 x 10-bit (single channel)
  - 1,036,800 x 12-bit (single channel)
  - 777,600 x 16-bit (single channel)
  - 622,080 x 20-bit (single channel)
  - 518,400 x 24-bit (single channel)
  - 777,600 x 8-bit (each of two parallel channels)
  - 622,080 x 10-bit (each of two parallel channels)
  - 518,400 x 12-bit (each of two parallel channels)
- ▶ User-Resettable Read and Write Pointers
- ▶ Choice of Control Interfaces:
  - Two-Wire Serial Microprocessor Interface
  - Eight-Wire Parallel Microprocessor Bus
- ▶ 3.3 Volt Power Supply
- ▶ 5 Volt Tolerant I/O
- ▶ 100-lead PQFP Package
- ▶ Industrial Temperature Available

<sup>(a)</sup> Power-up Default Mode

## Applications

- ▶ Field-Based or Frame-Based Comb Filtering
- ▶ Image or Data Sequence Capture
- ▶ Resynchronization of Data Streams
- ▶ Video Special Effects:
  - Rotation, Zoom, Picture-in-Picture
- ▶ Test Pattern Generation
- ▶ Motion Detection or Frame-to-Frame Correlation
- ▶ Closed Circuit of Security Camera Systems

## LF3312 Functional Block Diagram



\* Doubles as lower portion of random address input  
 \*\* Doubles as upper portion of random address input or as parallel microprocessor port

## Features

- ▶ 100 MHz Operation
- ▶ 16-bit Fixed Point Data Precision (96 dB Dynamic Range) on Output with 20-bit Internal Computation Precision
- ▶ Computes up to a 1024 Point Complex FFT in 18  $\mu$ s\* using a Single Processor
- ▶ 4 Programmable Complex FFT Point Sizes: 16 Point (240 ns), 64 Point (1.2  $\mu$ s), 256 Point (3.4  $\mu$ s), and 1024 Point (18  $\mu$ s)\*\*
- ▶ Supports Both Forward and Inverse Fast Fourier Transforms
- ▶ Configurable as a FIR Filter with up to 1024 Complex Taps
- ▶ Contains Seven Built-In Windowing Functions in ROM
- ▶ Window Buffer (2K x 16-bit) Enables Users to Program Their Own Complex Window Functions Through Independent Address and Data Input Lines
- ▶ Standby Modes Result in Significant Power Savings While Simultaneously Retaining Internal Memory Data

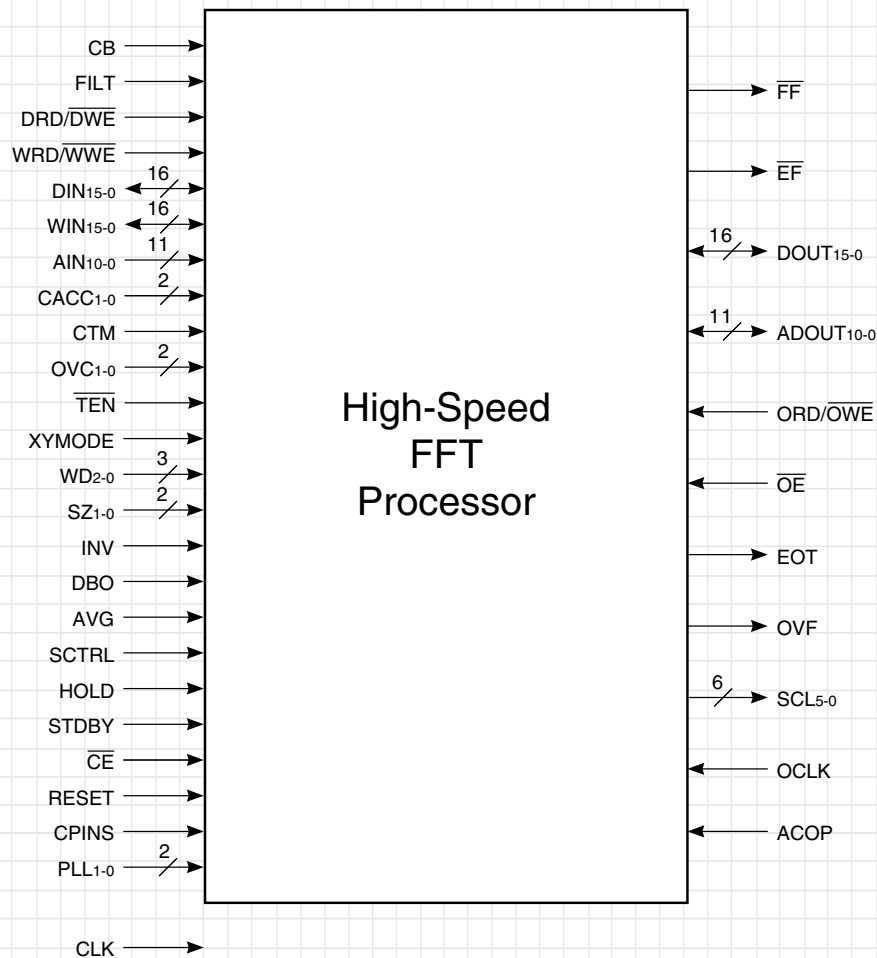
- ▶ 224K-bit Internal RAM
- ▶ 1.5M-bit Internal Function ROM
- ▶ 3.3 Volt Power Supply
- ▶ 5 Volt Tolerant I/O
- ▶ 160-pin PQFP Package
- ▶ Industrial Temperature Available

\* 1024 Complex FFT Computation Time Based on XY Mode with 25% Input Overlap. 1024 Complex FFT with No Overlap and Averaged Linear or Decibel Power is Computed in 24  $\mu$ s.

\*\* All Computation Times Based on XY Mode with 25% Input Overlap.

( Additional Comments on the Self Governing Processing Rate. The LF7710 starts processing once sufficient data has been loaded and stops processing when the finished data isn't being read fast enough. The Radix 4 processing architecture provides enhanced data rate. )

## LF7710 Functional Block Diagram

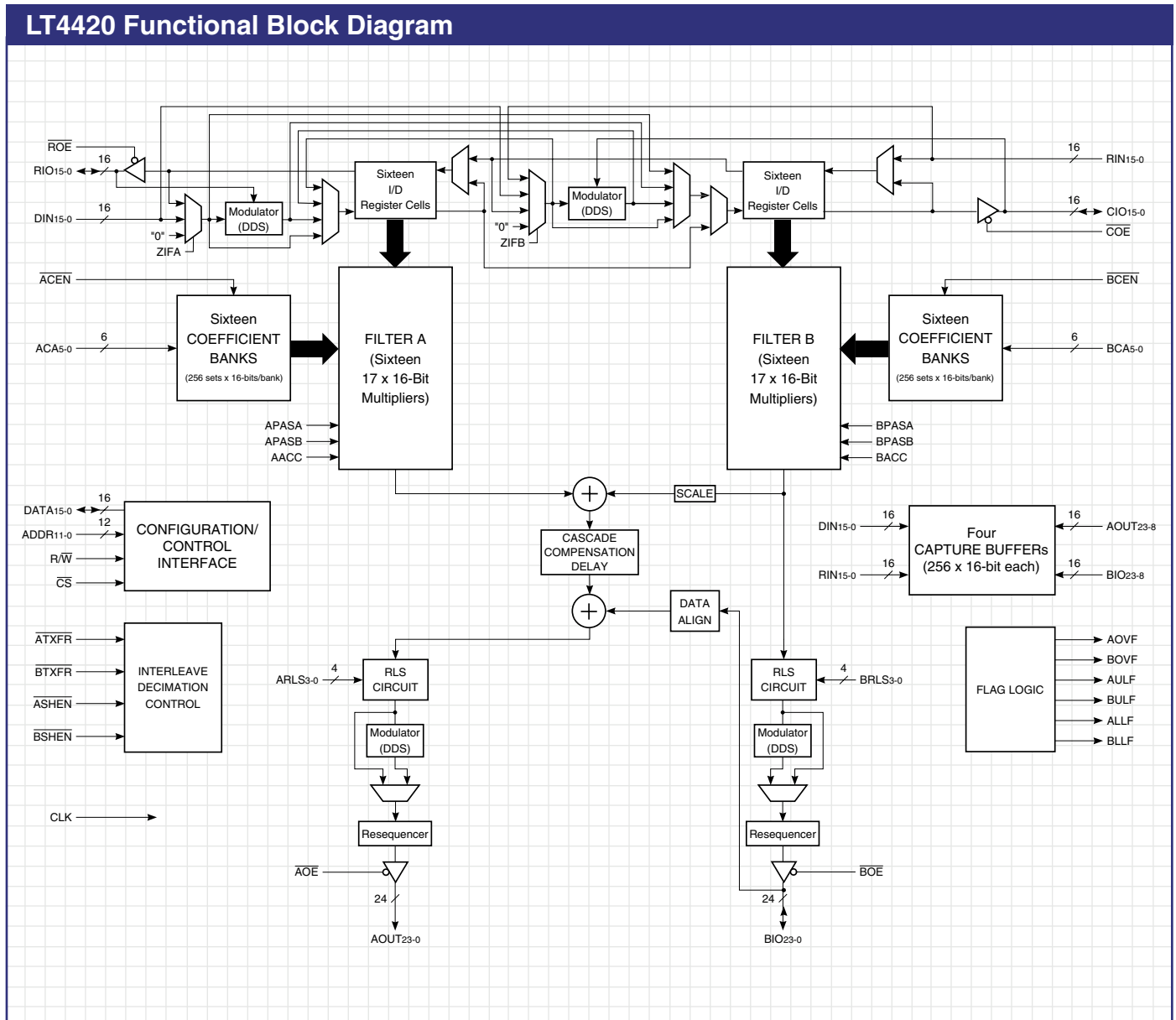


## Features

- ▶ 155 MHz Max Data Rate
- ▶ 312 MHz Max Core Clock Rate\*
- ▶ 16-bit Data and Coefficients Paths
- ▶ 64-Tap FIR Filter, Cascadable for More Filter Taps
- ▶ Various Operating Modes: Dual Filter, Single Filter, 32-Bit Data or Coefficient, Double Rate, Auto Decimate, Asymmetric Coefficient Set Expansion, and Matrix Multiplication
- ▶ Selectable 24-bit Data Output with User Defined Rounding and Limiting
- ▶ Supports up to 64 Interleaved Data Streams or a Decimation Factor up to 64:1 for Increasing Filter Taps
- ▶ Interleaved Accumulator Capability Adds Increased Flexibility When Interleaving
- ▶ 256 Filter Coefficients per Tap
- ▶ Built-in Cascade Ports Allow up to 16 Devices to be Cascaded without Any Additional Hardware
- ▶ Pre/Post-Modulator Stage with Built-In User-Programmable DDS (32-bit Accumulator)
- ▶ Auto Decimation Mode Eliminates the Need for External Coefficient, Transfer and Accumulator Controllers
- ▶ 1K Word by 16-bit Capture Buffer. Supports the Microcontroller When Calculation of New Coefficients is Required for Adaptive Filtering
- ▶ Microcontroller Interface
- ▶ 3.3 Volt Power Supply
- ▶ BGA Package to be Determined
- ▶ Industrial Temperature Available

\* 312 MHz is a Target Spec Only and is Process Related.

### LT4420 Functional Block Diagram



Imaging Products						
Device	Product	Bits	Pin/Package Options		Voltage	Speed (ns)
LF2242	Half-Band Digital Filter	12	44L. PLCC	44L. PQFP	5	25
LF2246	Image Filter	10	120L. PQFP		5	15
LF2247	Image Filter w/ Coefficient RAM	10	84L. PLCC	100L. PQFP	5	15
LF2249	Digital Mixer	12	120L. PQFP		5	25
LF2250	Matrix Multiplier	10	120L. PQFP		5	20
LF2272	Colorspace Converter	12	120L. PQFP		5	20
LF2301	Image Resampling Sequencer		68L. PLCC		5	25
LF3304	Dual 4K Line Buffer / FIFO	12	100L. PQFP		3.3	10
LF3310	Horizontal/Vertical Digital Image Filter	12	144L. PQFP		3.3	12
LF3320	Horizontal Digital Image Filter	12	144L. PQFP		3.3	12
LF3330	Vertical Digital Image Filter	12	100L. PQFP		3.3	12
LF3338	Vertical Digital Image Filter	8	100L. PQFP		3.3	12
LF3347	High Speed Image Filter w/ Coefficient RAM	12	120L. PQFP		3.3	12
LF3370	High Definition Video Format Converter	13	160L. PQFP		3.3	12
LF43168	Dual 8-Tap FIR Filter	10	84L. PLCC	100L. PQFP	5	15
LF43881	Digital Filter	8	84L. PLCC		5	40
LF43891	Digital Filter	9	84L. PLCC		5	33
LF48212	Alpha Mixer	12	68L. PLCC	64L. PQFP	5	20
LF48410	Video Histogrammer	24	84L. PLCC		5	25
LF48908	Two Dimensional Convolver	8	84L. PLCC	100L. PQFP	5	25
LF9501	1K Line Buffer	10	44L. PLCC		5	20
LF9502	2K Line Buffer	10	44L. PLCC		5	20

Multipliers						
Device	Product	Bits	Pin/Package Options		Voltage	Speed (ns)
LMU08	Signed	8	44L. PLCC	40L. DIP	5	35
LMU8U	Unsigned	8	44L. PLCC	40L. DIP	5	35
LMU18	32 Outputs	16	84L. PLCC		5	35
LMU112	Reduced Pin out	12	52L. PLCC	48L. DIP	5	25
LMU216	Surface mount	16	68L. PLCC		5	20
LMU217	Microprogram, Surface Mount	16	68L. PLCC		5	25

Multiplier - Accumulators						
Device	Product	Bits	Pin/Package Options		Voltage	Speed (ns)
LMA2009	Surface Mount	12	68L. PLCC		5	20
LMA2010	Surface Mount	16	68L. PLCC		5	25

### Arithmetic Logic Units

Device	Product	Bits	Pin/Package Options	Voltage	Speed (ns)
L4C381	Cascadable ALU	16	68L. PLCC	5	15
L4C383	Cascadable ALU (Extended Set)	16	68L. PLCC	5	20

### Special Arithmetic Functions

Device	Product	Bits	Pin/Package Options	Voltage	Speed (ns)
LSH32	Barrel Shifter	32	68L. PLCC	5	20
LSH33	Barrel Shifter w / Registers	32	68L. PLCC	5	30
L2330	Coordinate Transformer	24	120L. PQFP	5	20
L2340	Digital Synthesizer	24	120L. PQFP	5	20

### Pipeline Registers

Device	Product	Bits	Pin/Package Options	Voltage	Speed (ns)
L10C11	Variable Length (3-18 Stages)	8	28L. PLCC 24L. DIP	5	15
L29C520	Multilevel (1-4 Stages)	8	28L. PLCC 24L. DIP	5	22
L29C521	Multilevel (1-4 Stages)	8	28L. PLCC 24L. DIP	5	22
L29C525	Dual 8 Deep (1-16)	8	28L. PLCC 28L. DIP	5	15
LPR520	Multilevel (1-4 Stages)	16	44L. PLCC 40L. DIP	5	22

### Multiplier - Summers

Device	Product	Bits	Pin/Package Options	Voltage	Speed (ns)
LMS12	Plus 26 bit FIR	12	84L. PLCC	5	35

### Product Ordering Information\*

Prefix, LOGIC Devices Inc. ——— **LF** **3320** **Q** **C** **12**

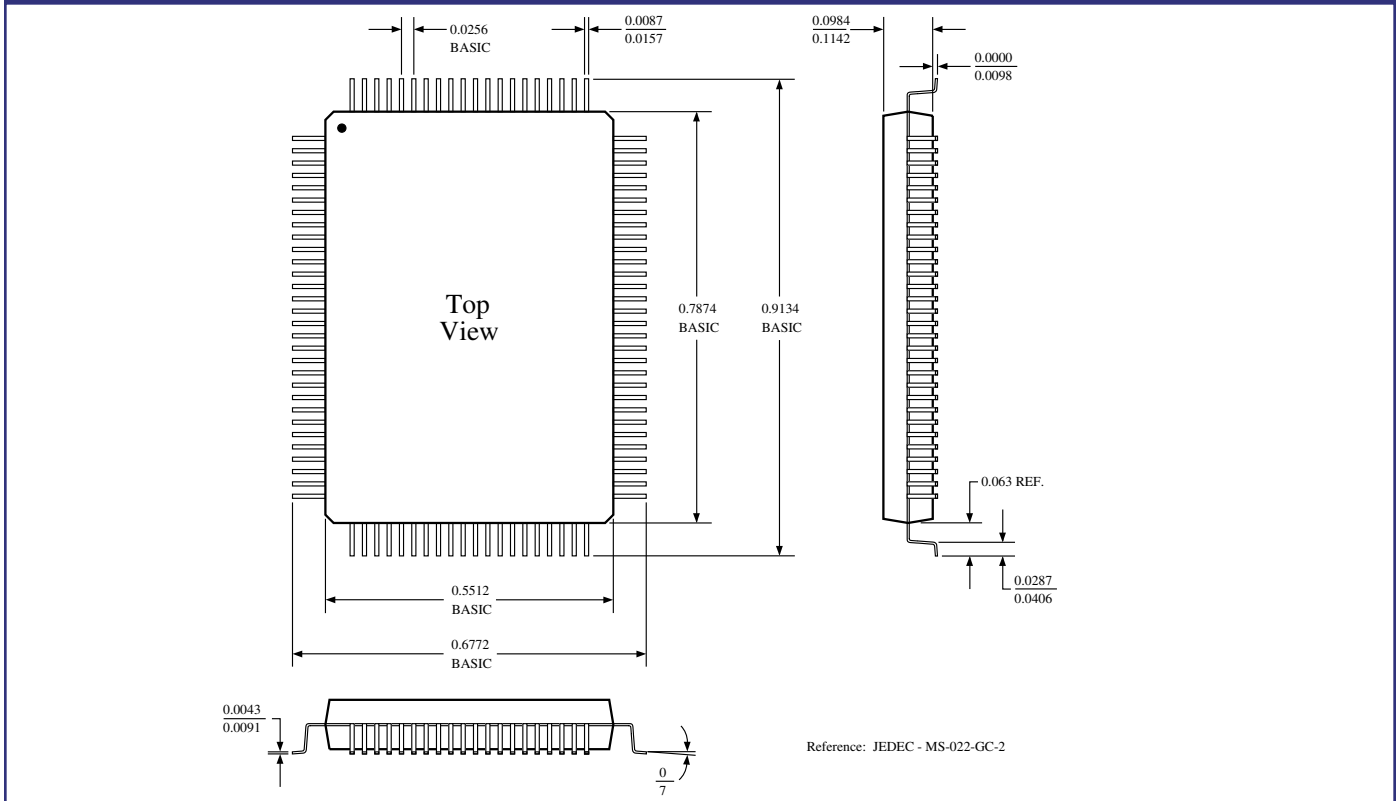
Device Number ——— Performance/Speed Range

Package Codes	
Suffix	Description
J	Plastic J-Lead Chip Carrier
P	Plastic DIP
Q	Plastic Quad Flatpack

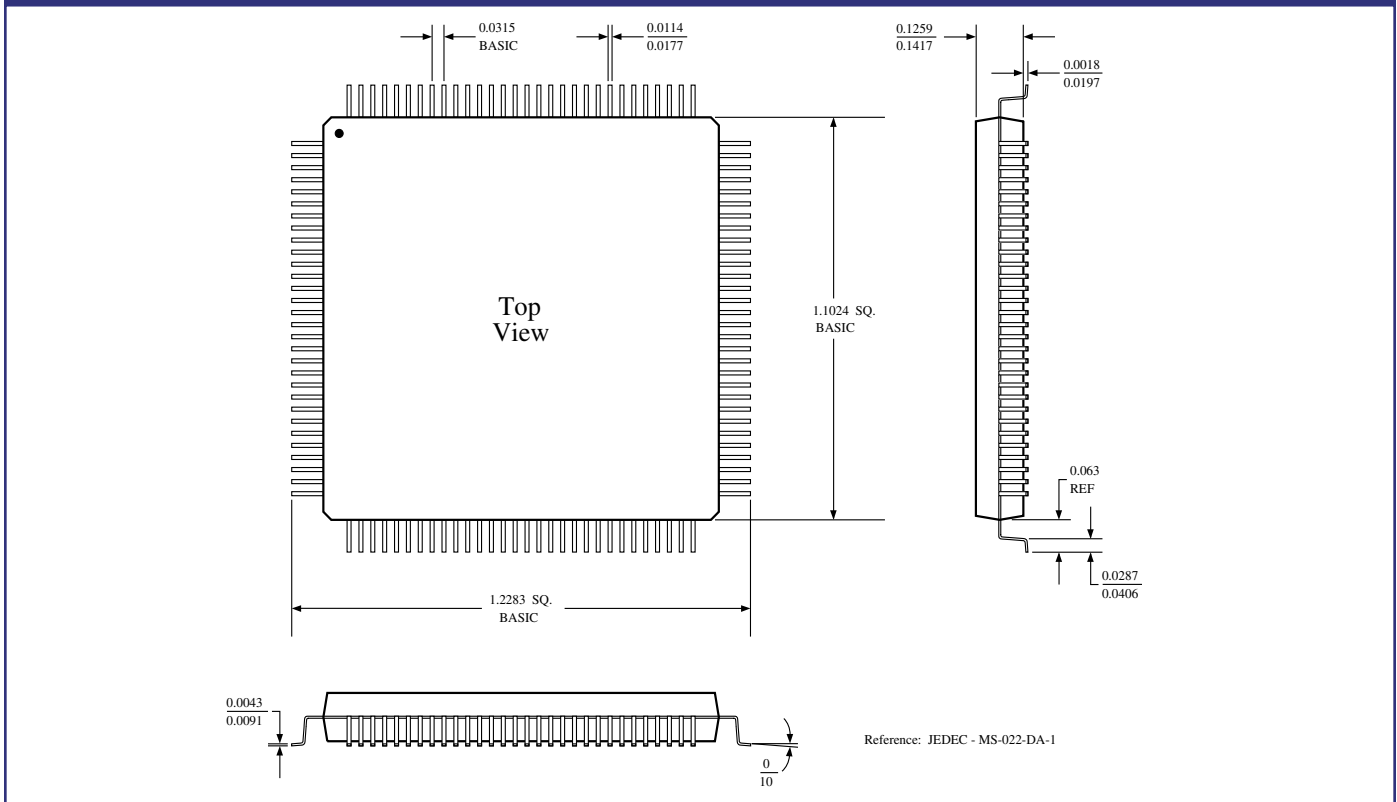
Temperature Range	
Suffix	Description
C	Commerical 0°C to +70°C
I	Industrial -40°C to +85°C

\*The Product Ordering Information Table on the last page of each data sheet indicates most valid combination of package, temperature, and performance codes for a given product. Please check our web site at <http://www.logicdevices.com> for the latest data.

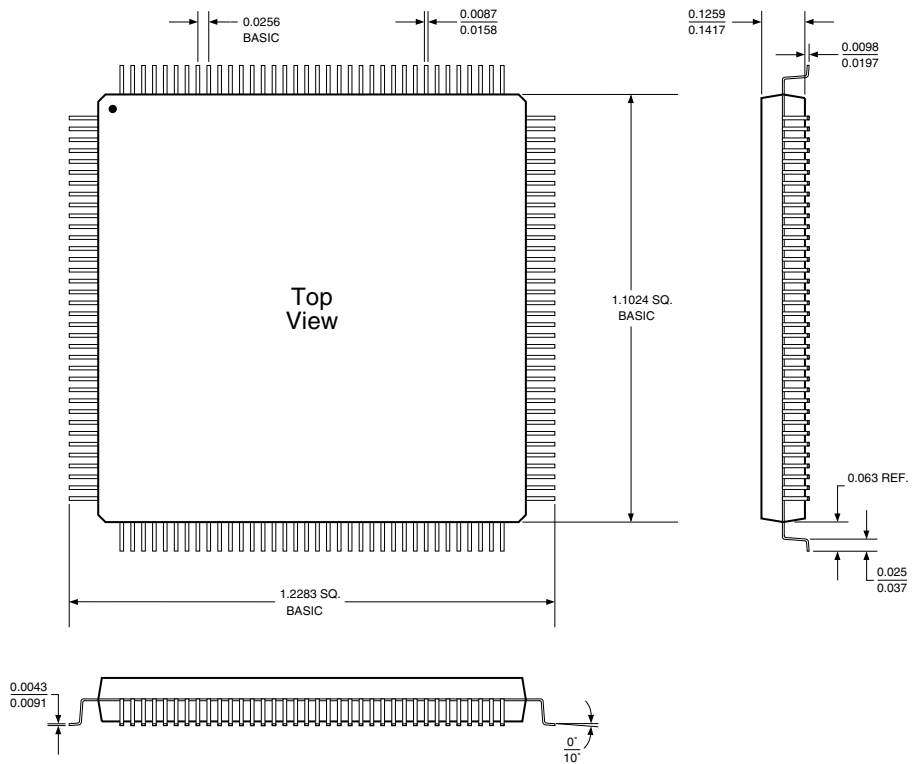
**100-pin Plastic Quad Flatpack (Ordering Code: Q)**



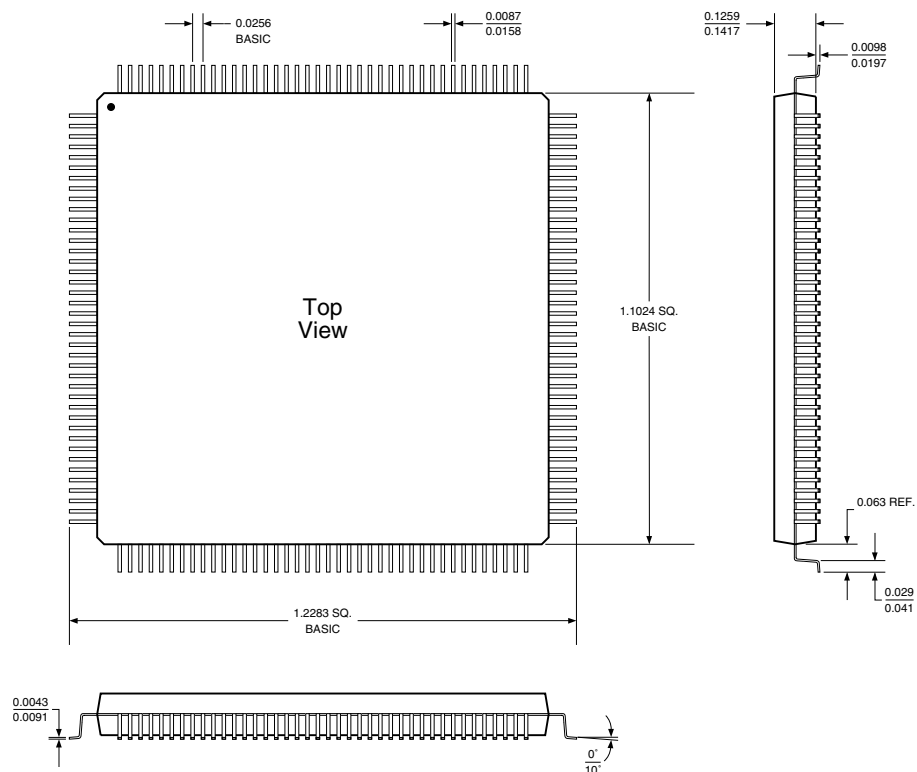
**120-pin Plastic Quad Flatpack (Ordering Code: Q)**



**144-pin Plastic Quad Flatpack (Ordering Code: Q)**



**160-pin Plastic Quad Flatpack (Ordering Code: Q)**



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